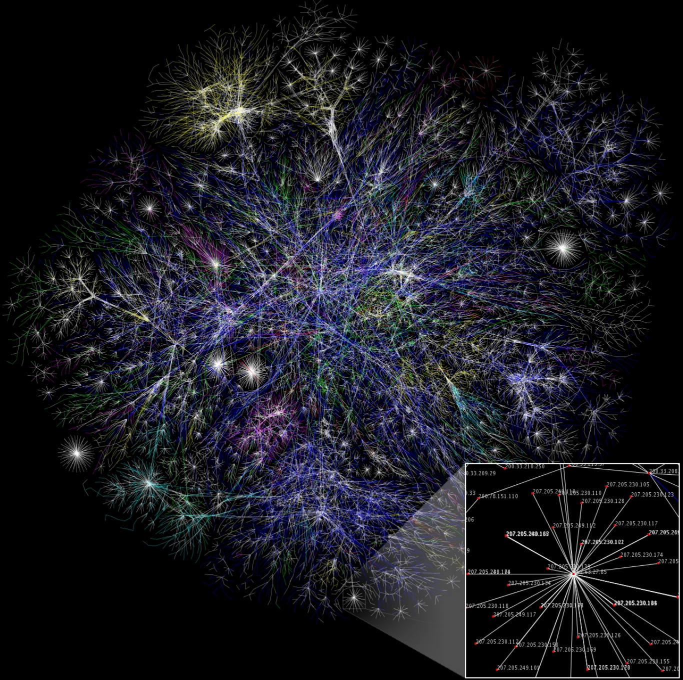
Cloud Operating Systems

Daniel Gruss

2023-03-01



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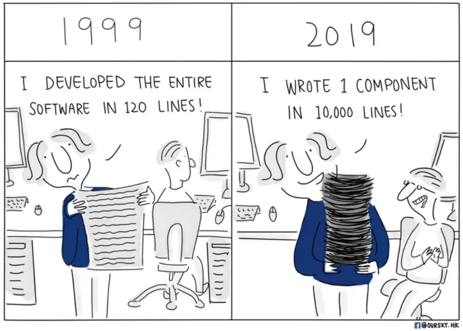
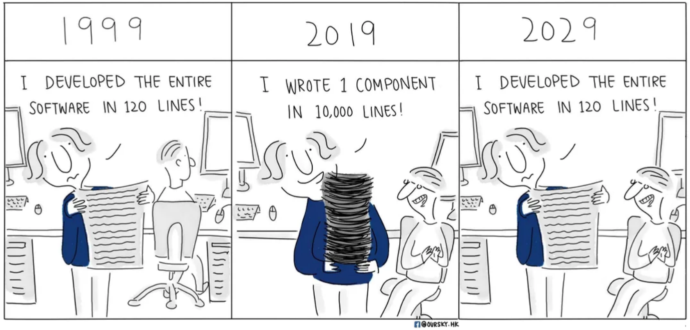

1999
2019
I DEVELOPED THE ENTIRE SOFTWARE IN 120 LINES!
I WROTE 1 COMPONENT IN 10,000 LINES!
@OURSKY.HK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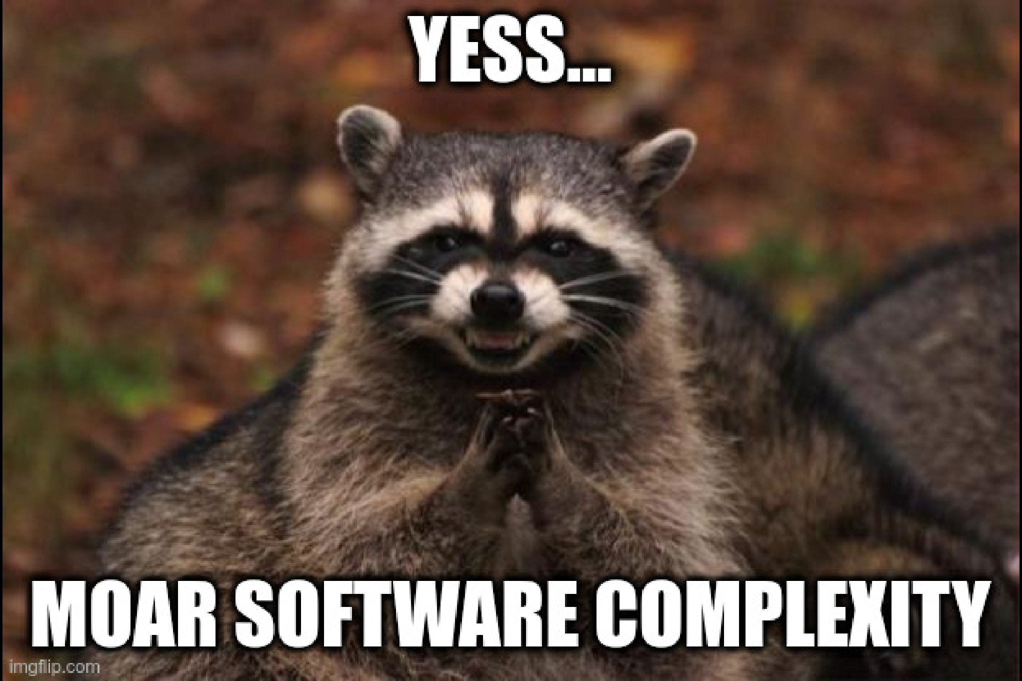
YESS...
MOAR SOFTWARE COMPLEXITY
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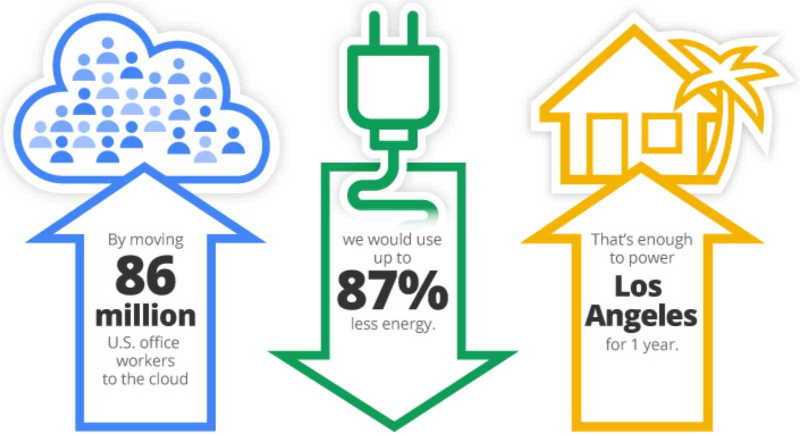
Moving to the cloud can save up to 87% of IT energy



Cloud means Efficiency

How does the cloud bring efficiency?

Apply OS techniques - Example?

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→ Let other processes run in between

IaaS
PaaS
SaaS

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- Isolation of tenants (security, reliability, availability)
- Abstraction of hardware

What is Virtualization?

Virtualization allows to represent resources in a computer in a way they can be used easily and without the need to know details of their properties

Virtual Machines (VM)

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- OS does not know if HW is concurrently used by other VMS

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  - multiple servers on one box

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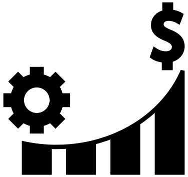

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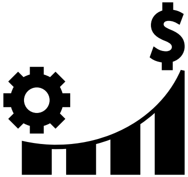

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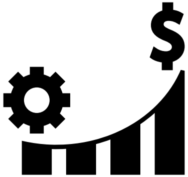

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- simple migration to more powerful hardware

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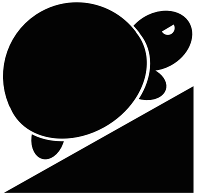

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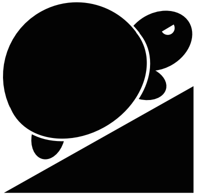

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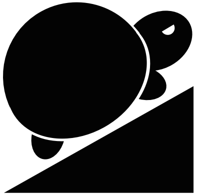

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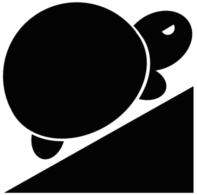

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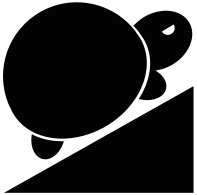

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Modern Virtualization

- OS-level Virtualization

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- Para-Virtualization

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- examples: OpenVZ, Docker, (s)chroot

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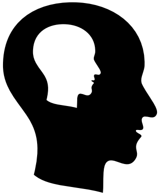

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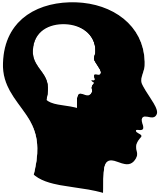

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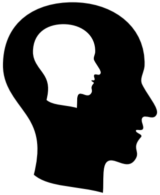

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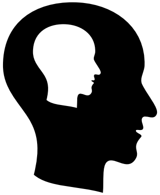

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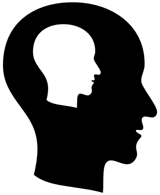

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- not usable for closed source OSes

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  - every physical component has to be virtualized and requires drivers in OS

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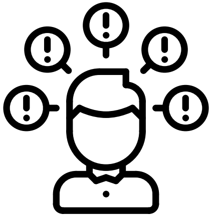

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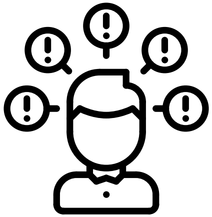

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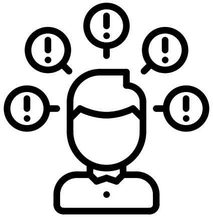

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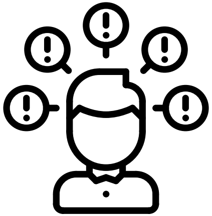

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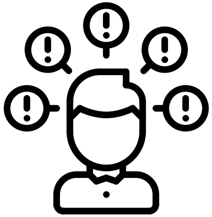

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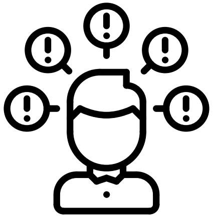

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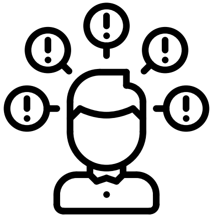

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- Access to these areas not allowed for guest. Invokes switch to hypervisor who has to emulate these accesses

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- forwarding of virtual interrupts must consider IF

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- cannot be saved and restored when switching between VMs

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        - supports VMs
- Both modes have ring 0-3

Intel Virtualization Architecture

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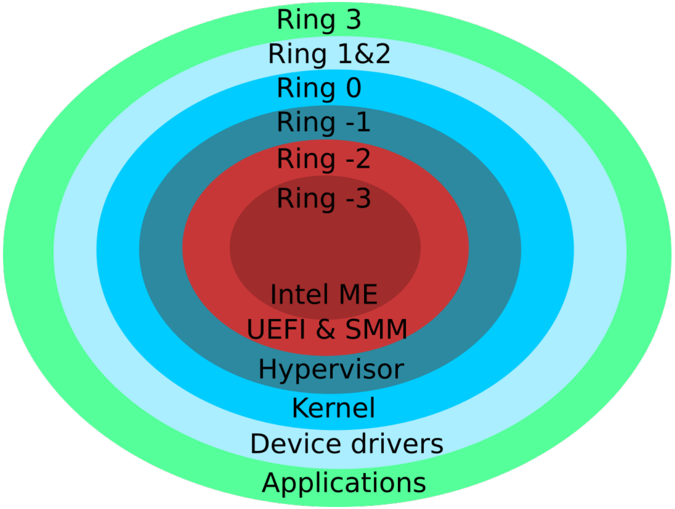
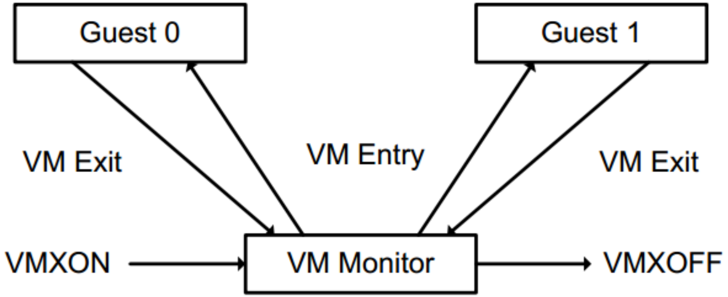
- guest can run in ring 0
- hypervisor said to be running in “ring -1”

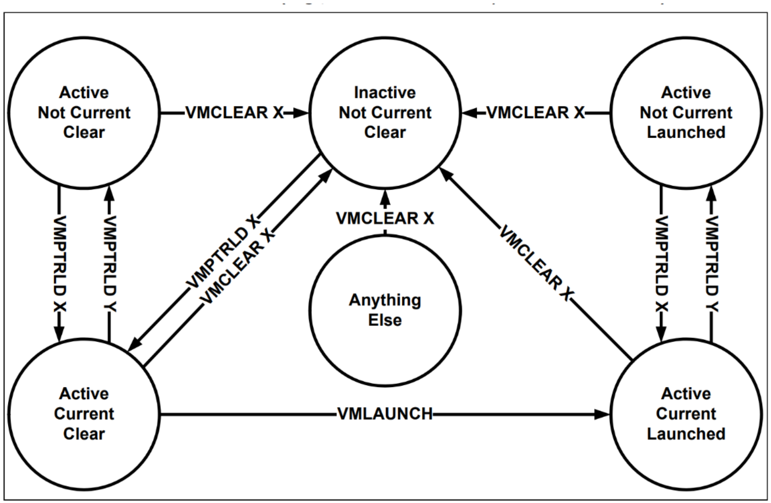
Rings on Intel



VMM Operation



VMM Transitions



VT-x

- VM entry: root operation $\rightarrow$ non-root operation

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VT-x

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- VM exit: non-root operation $\rightarrow$ root operation
- VMCS: Virtual Machine Control Structure
    - Guest-state-area
    - Host-state-area
- Entry/Exit loads/safes information using the proper area

VMCS - Guest State Area

- Contains elements comprising the state of the virtual CPU of a VMCS

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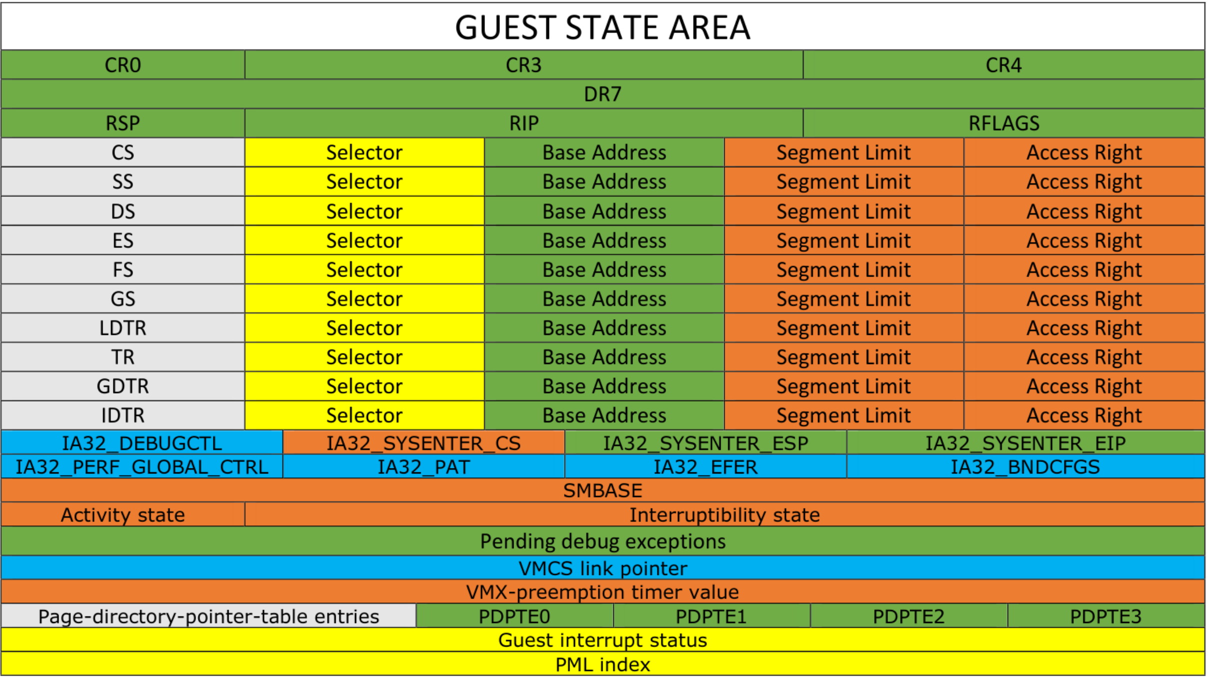
- VM-exit requires loading certain registers (like segment registers, CR3, IRTR...)
- GSA contains fields for these registers
- GSA contains fields for other information not readable via registers
    - e.g. interruptability state

- 🟩 Natural-Width fields.
- 🟨 16-bits fields.
- 🟧 32-bits fields.
- 🟦 64-bits fields.



GUEST STATE AREA

CR0	CR3		CR4	
DR7				
RSP	RIP		RFLAGS	
CS	Selector	Base Address	Segment Limit	Access Right
SS	Selector	Base Address	Segment Limit	Access Right
DS	Selector	Base Address	Segment Limit	Access Right
ES	Selector	Base Address	Segment Limit	Access Right
FS	Selector	Base Address	Segment Limit	Access Right
GS	Selector	Base Address	Segment Limit	Access Right
LDTR	Selector	Base Address	Segment Limit	Access Right
TR	Selector	Base Address	Segment Limit	Access Right
GDTR	Selector	Base Address	Segment Limit	Access Right
IDTR	Selector	Base Address	Segment Limit	Access Right
IA32_DEBUGCTL	IA32_SYSENTER_CS	IA32_SYSENTER_ESP	IA32_SYSENTER_EIP	
IA32_PERF_GLOBAL_CTRL	IA32_PAT	IA32_EFER	IA32_BNDCFGS	
SMBASE				
Activity state	Interruptibility state			
Pending debug exceptions				
VMCS link pointer				
VMX-preemption timer value				
Page-directory-pointer-table entries	PDPTE0	PDPTE1	PDPTE2	PDPTE3
Guest interrupt status				
PML index				

HOST STATE AREA

CR0	CR3	CR4
RSP	RIP	
CS	Selector	
SS	Selector	
DS	Selector	
ES	Selector	
FS	Selector	Base Address
GS	Selector	Base Address
TR	Selector	Base Address
GDTR	Base Address	
IDTR	Base Address	
IA32_SYSENTER_CS	IA32_SYSENTER_ESP	IA32_SYSENTER_EIP
IA32_PERF_GLOBAL_CTRL	IA32_PAT	IA32_EFER

VMCS

- Addressed using physical addresses

VMCS

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- not part of guest address space

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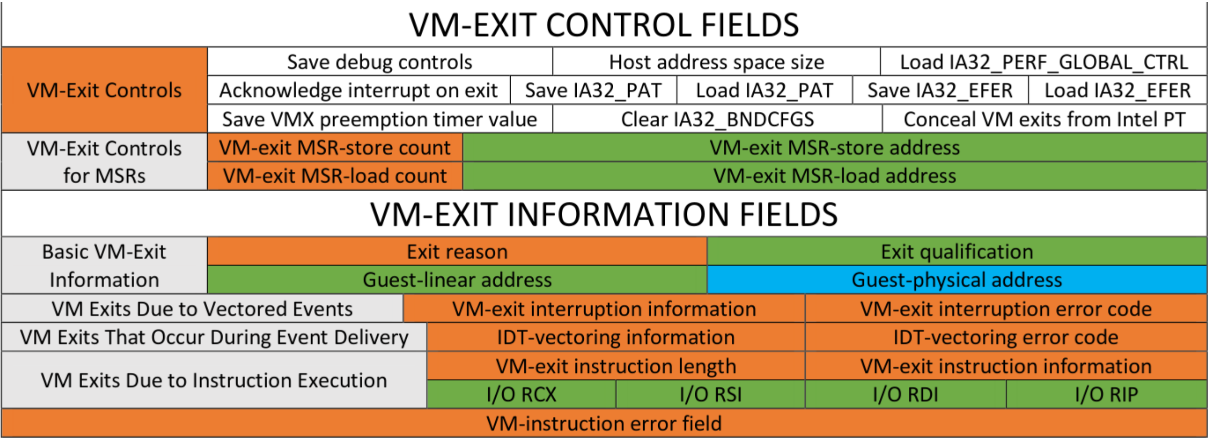
  - exit reason
  - exit qualification



VM-EXIT CONTROL FIELDS

VM-Exit Controls	Save debug controls		Host address space size		Load IA32_PERF_GLOBAL_CTRL
	Acknowledge interrupt on exit	Save IA32_PAT	Load IA32_PAT	Save IA32_EFER	Load IA32_EFER
	Save VMX preemption timer value		Clear IA32_BNDCFGS		Conceal VM exits from Intel PT
VM-Exit Controls for MSRs	VM-exit MSR-store count	VM-exit MSR-store address			
	VM-exit MSR-load count	VM-exit MSR-load address			

VM-EXIT INFORMATION FIELDS

Basic VM-Exit Information	Exit reason		Exit qualification	
	Guest-linear address		Guest-physical address	
VM Exits Due to Vectored Events	VM-exit interruption information		VM-exit interruption error code	
VM Exits That Occur During Event Delivery	IDT-vectoring information		IDT-vectoring error code	
VM Exits Due to Instruction Execution	VM-exit instruction length		VM-exit instruction information	
	I/O RCX	I/O RSI	I/O RDI	I/O RIP
VM-instruction error field				

VMCS

- Example: MOV CR

VMCS

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VMCS

- Example: MOV CR
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- Exit qualification:
    - which CR
    - direction (Rx→CR or CR→Rx)
    - register used

CONTROL FIELDS

Pin-Based VM-Execution Controls	External-interrupt exiting	NMI exiting	Virtual NMIs	
	Activate VMX-preemption timer	Process posted interrupts		
Primary processor-based VM-execution controls	Interrupt-window exiting	Use TSC offsetting		
	HLT exiting	INVLPG exiting	MWAIT exiting	RDPMC exiting
	RDTSC exiting	CR3-load exiting	CR3-store exiting	CR8-load exiting
	CR8-store exiting	Use TPR shadow	NMI-window exiting	MOV-DR exiting
	Unconditional I/O exiting	Use I/O bitmaps	Monitor trap flag	Use MSR bitmaps
	MONITOR exiting	PAUSE exiting	Activate secondary controls	
Secondary processor-based VM-execution controls	Virtualize APIC accesses	Enable EPT	Descriptor-table exiting	Enable RDTSCP
	Virtualize x2APIC mode	Enable VPID	WBINVD exiting	Unrestricted guest
	APIC-register virtualization	Virtual-interrupt delivery	PAUSE-loop exiting	
	RDRAND exiting	Enable INVPCID	Enable VM functions	VMCS shadowing
	Enable ENCLS exiting	RDSEED exiting	Enable PML	EPT-violation #VE
	Conceal VMX non-root operation from Intel PT	Enable XSAVES/XRSTORS		
	Mode-based execute control for EPT	Use TSC scaling		
Exception Bitmap	I/O-Bitmap Addresses	TSC-offset		
Guest/Host Masks for CR0	Guest/Host Masks for CR4	Read Shadows for CR0	Read Shadows for CR4	
CR3-target value 0	CR3-target value 1	CR3-target value 2	CR3-target value 3	CR3-target count
APIC Virtualization	APIC-access address	Virtual-APIC address	TPR threshold	
	EOI-exit bitmap 0	EOI-exit bitmap 1	EOI-exit bitmap 2	EOI-exit bitmap 3
	Posted-interrupt notification vector	Posted-interrupt descriptor address		
Read bitmap for low MSRs	Read bitmap for high MSRs	Write bitmap for low MSRs	Write bitmap for low MSRs	
Executive-VMCS Pointer	Extended-Page-Table Pointer	Virtual-Processor Identifier		
PLE_Gap	PLE_Window	VM-function controls	VMREAD bitmap	VMWRITE bitmap
ENCLS-exiting bitmap	PML address			
Virtualization-exception information address	EPTP index	XSS-exiting bitmap		

Virtualization: Trend 2000s $\rightarrow$ 2010s

The next step ($\approx$ 2005):

- Virtualization Hardware Extensions for Intel and AMD

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$\rightarrow$ IaaS VMs become widely used

Hardware Exentions: Intel VT

- Support for interrupt-virtualization

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    - VM-exit with any change of these registers
    - can be set on which bits this shall happen

Solves our problems

- Address Space Compression

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    - change of address space with any switch guest/hypervisor

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  - change of address space with any switch guest/hypervisor
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- Ring Problems, SYSENTER/SYSEXIT
  - Guest can now run in ring 0

Solves our problems

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- Hidden State

Solves our problems

- Non-faulting Access to Privileged State
  - access raise fault into hypervisor
- Hidden State
  - Saved into VMCS

Hypervisor and Virtual Memory

- Hypervisor uses virtual memory

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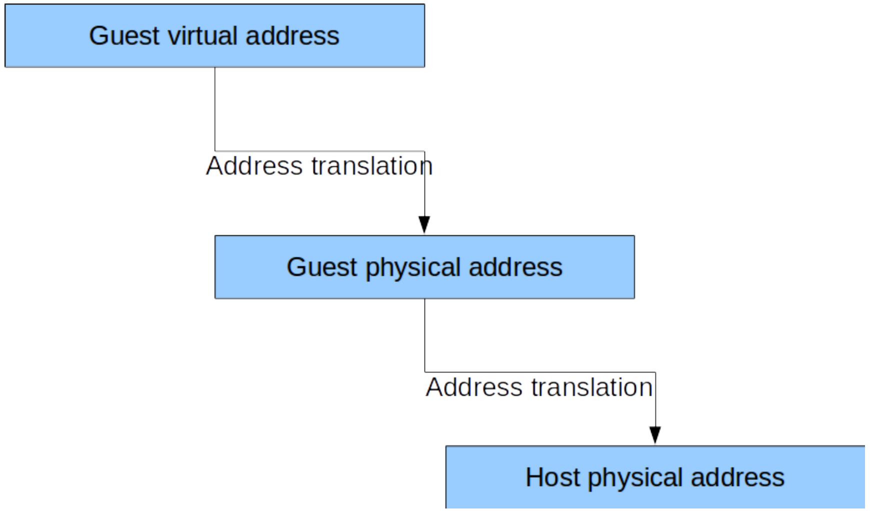
Virtual Memory



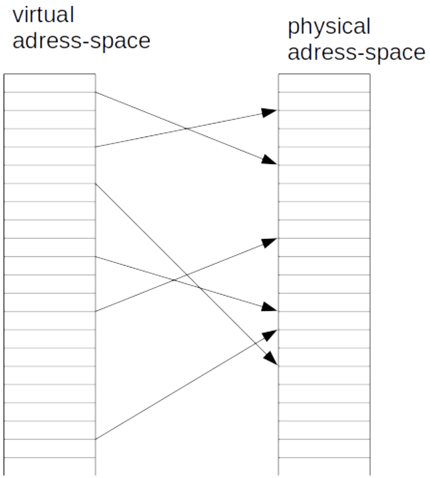
All problems in computer science can be solved by another level of indirection.

All problems in computer science can be solved by another level of indirection.

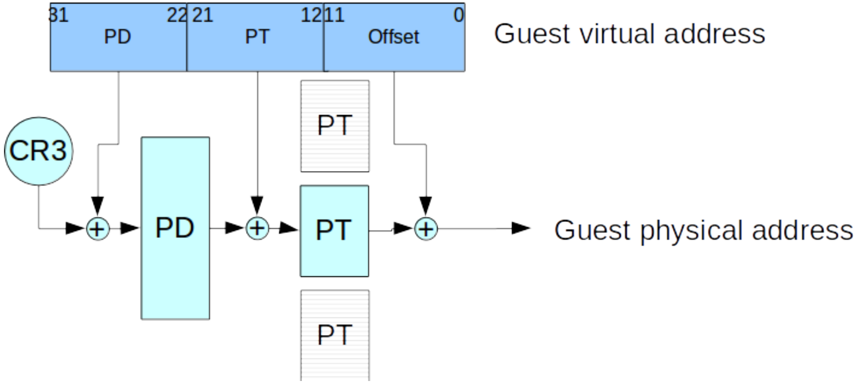
But that usually will create another problem.

David Wheeler

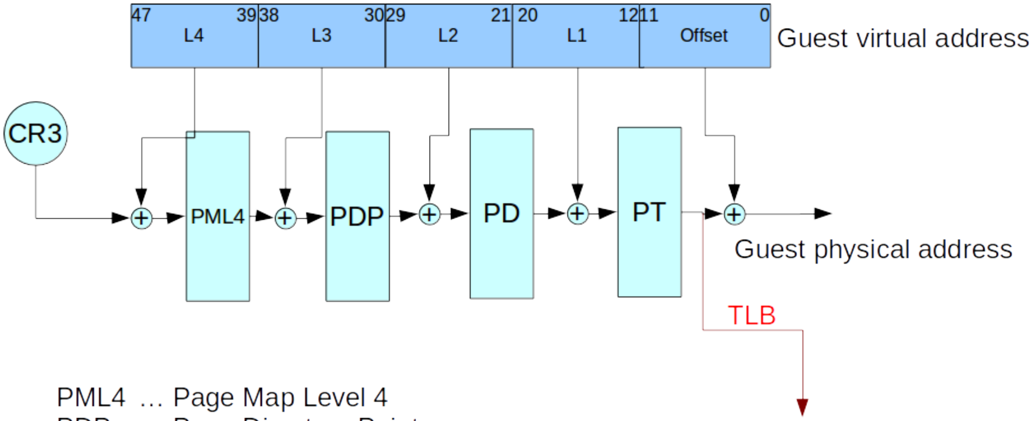
Paging



Known from theory and practice

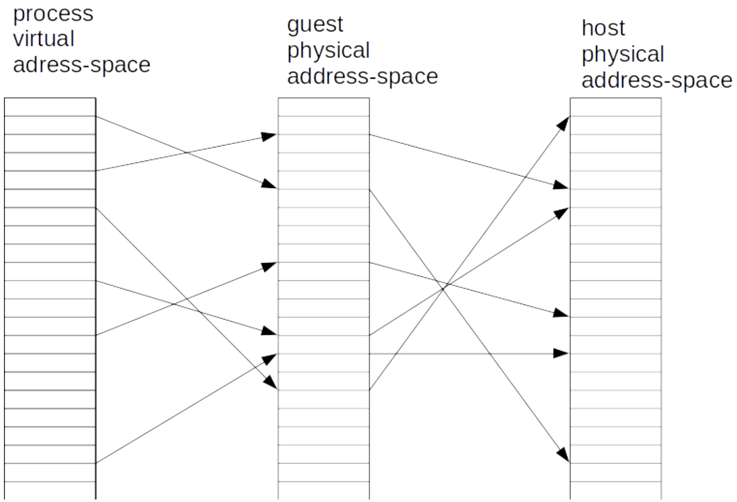


and in 64 bit...

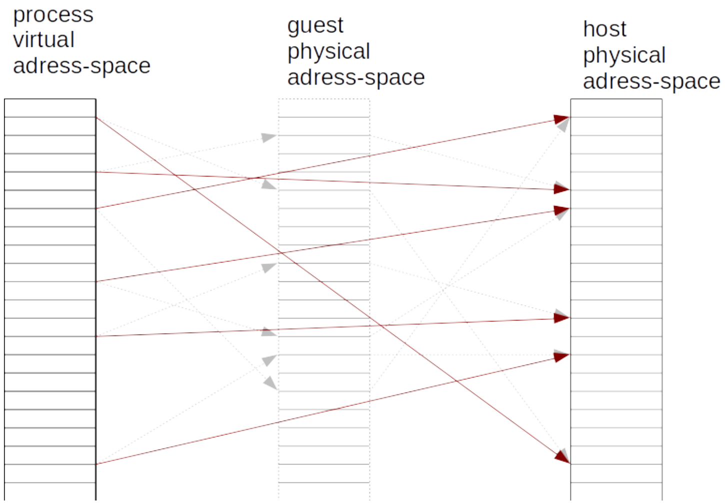


PML4	… Page Map Level 4
PDP	… Page Directory Pointer
PD	… Page Directory
PT	… Page Table

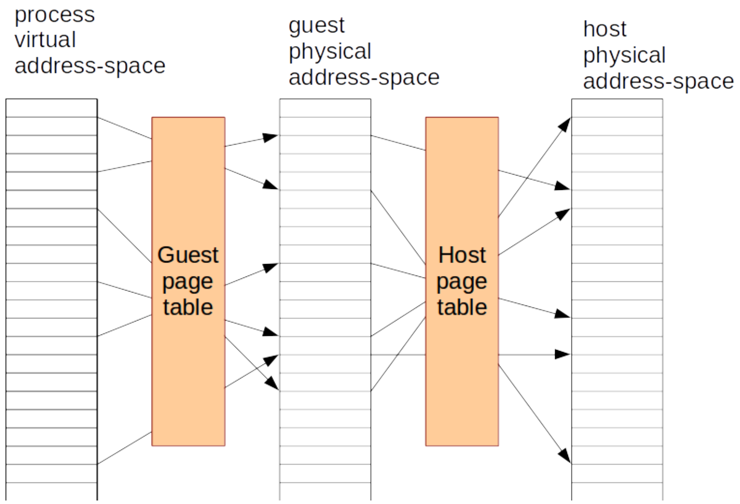
Combined Paging



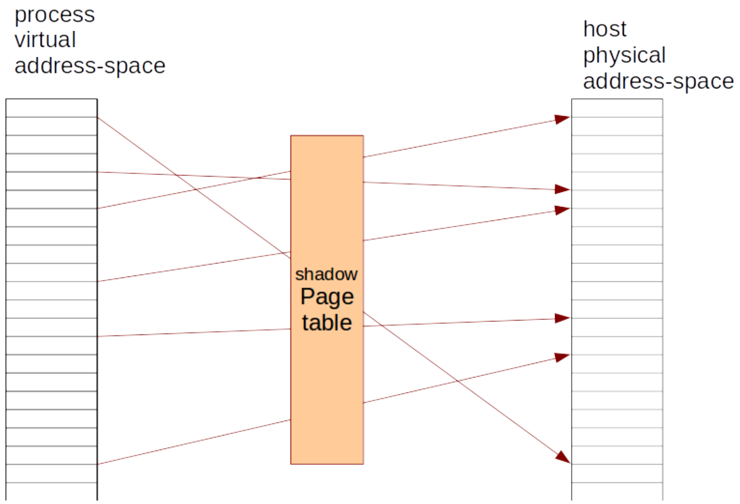
Shadow Page Table



Page Tables


process
virtual
address-space
guest
physical
address-space
host
physical
address-space
Guest
page
table
Host
page
table

Shadow Page Table



Shadow Page Table

- **merges** both page tables into one that the HW uses

Shadow Page Table

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- when guest changes own page table

Shadow Page Table

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  - Hypervisor has to catch access

Shadow Page Table

- **merges** both page tables into one that the HW uses
- when guest changes own page table
  - Hypervisor has to catch access
  - update shadow page table

Shadow Page Table

- when HW changes shadow page table

Shadow Page Table

- when HW changes shadow page table
- update guest PT

Shadow Page Table

- when HW changes shadow page table
- update guest PT
    - expensive!

Shadow Page Table

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  - page faults caught by hypervisor

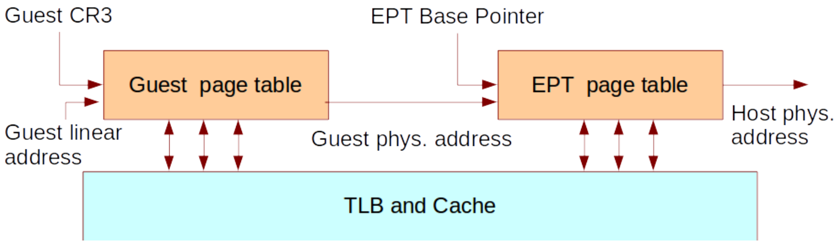
Shadow Page Table

- when HW changes shadow page table
- update guest PT
    - expensive!
    - page faults caught by hypervisor
    - must run through guest PTs

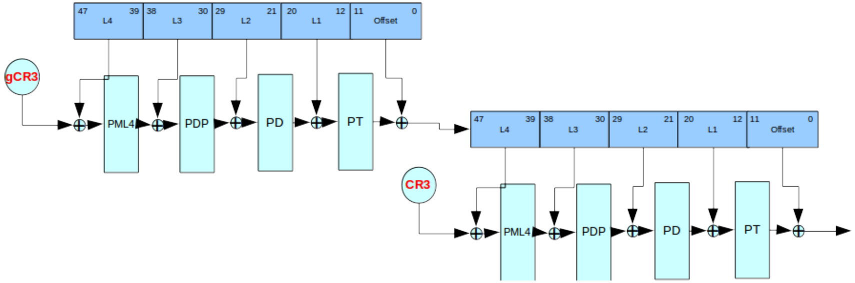
Shadow Page Table

- when HW changes shadow page table
- update guest PT
    - expensive!
    - page faults caught by hypervisor
    - must run through guest PTs
    - must emulate accessed and modified bits for guest

EPT


Guest CR3
EPT Base Pointer
Guest page table
EPT page table
Guest linear address
Guest phys. address
Host phys. address
TLB and Cache

Nested PT (NPT, AMD) / Extended PT (EPT, Intel)



“guest page walk”

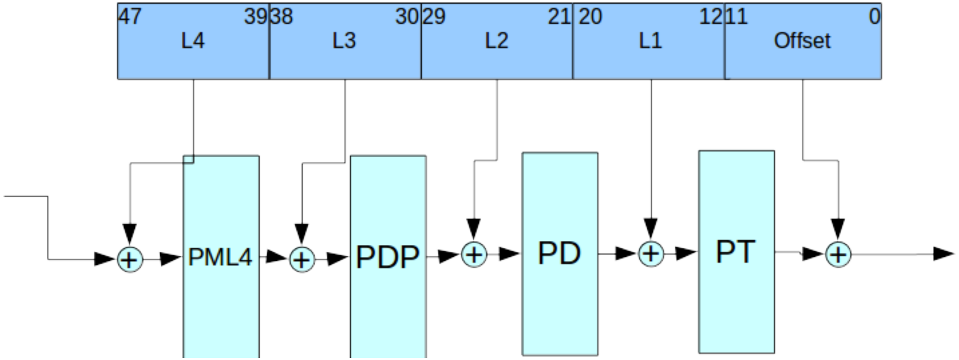
Guest page walk

- lots of memory accesses....

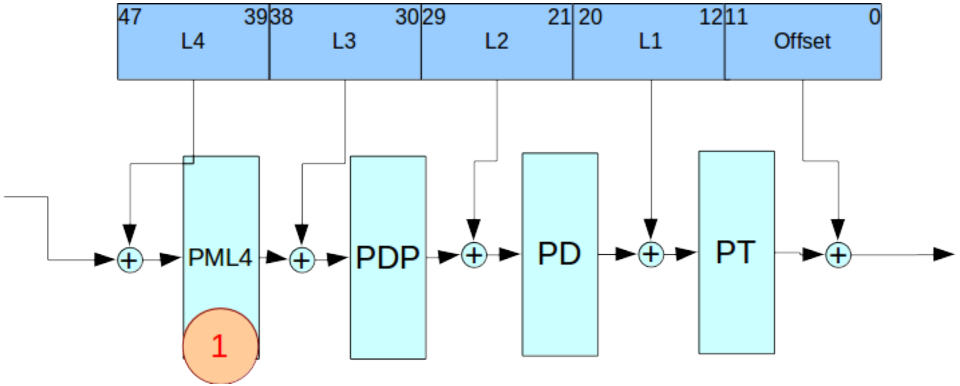
Guest page walk

- lots of memory accesses....
- but how many exactly?

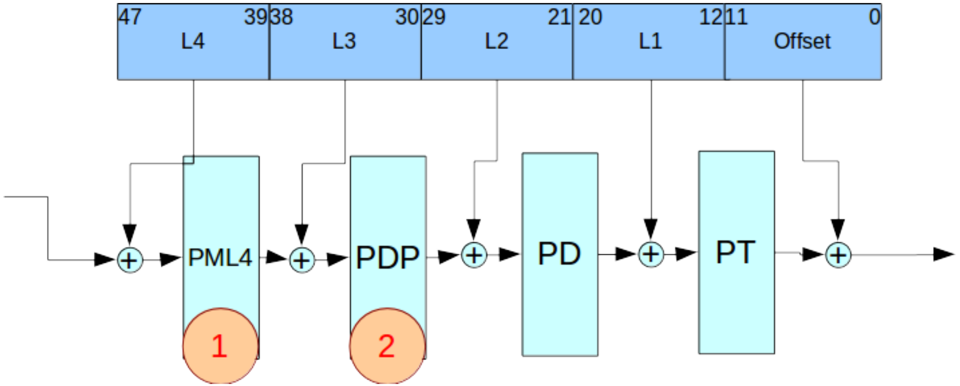
third for the host



third for the host



third for the host



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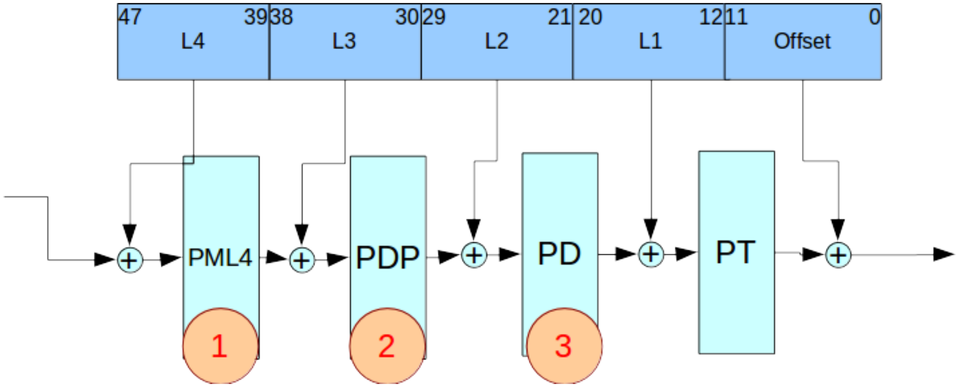

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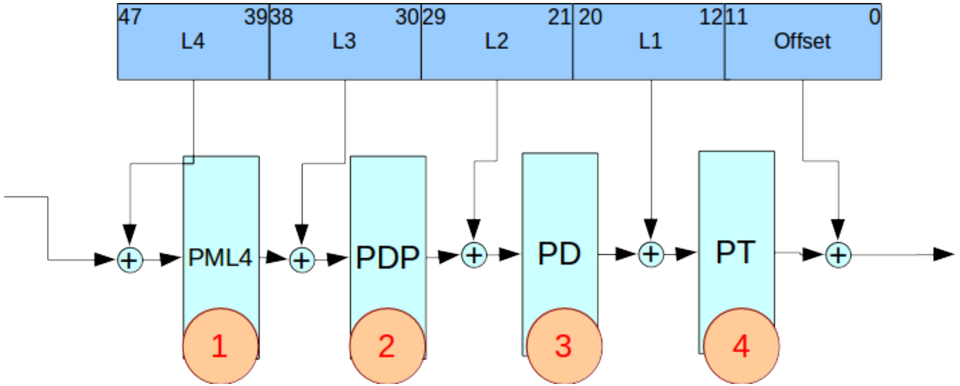
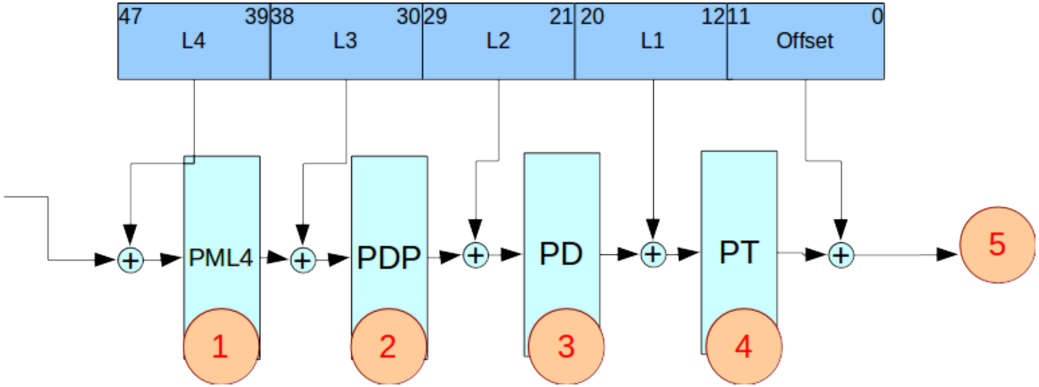
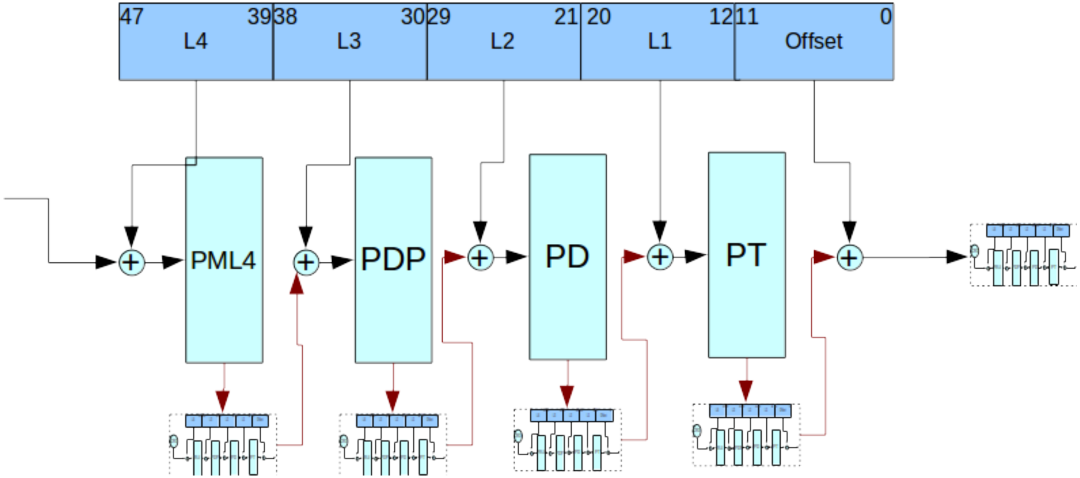


third for the host



And Combined



… and combined …

max. number of memory accesses per address translation

- 5 on guest level

… and combined …

max. number of memory accesses per address translation

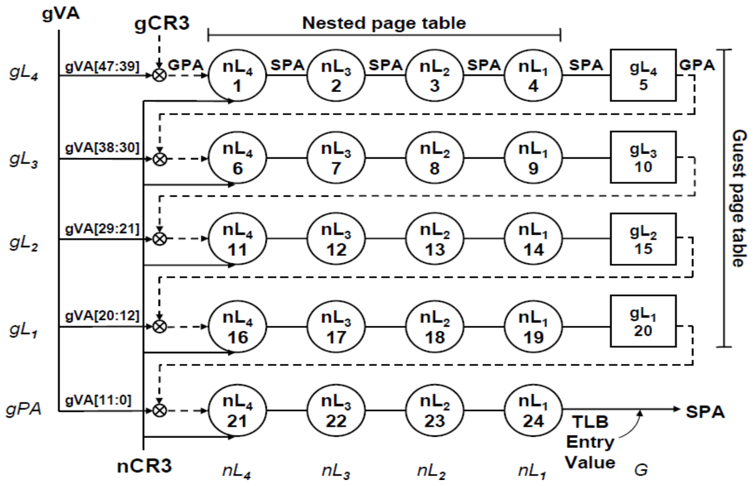
- 5 on guest level
- each induces 5 on host level

… and combined …

max. number of memory accesses per address translation

- 5 on guest level
- each induces 5 on host level
- makes 25!

Guest Page Walk



Performance

- depending on application: 3.9-4.6 times slower

Performance

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- but: TLB

Intel Features

- EPT only used if VM active

Intel Features

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- Translations tagged in TLB with EPT base pointer

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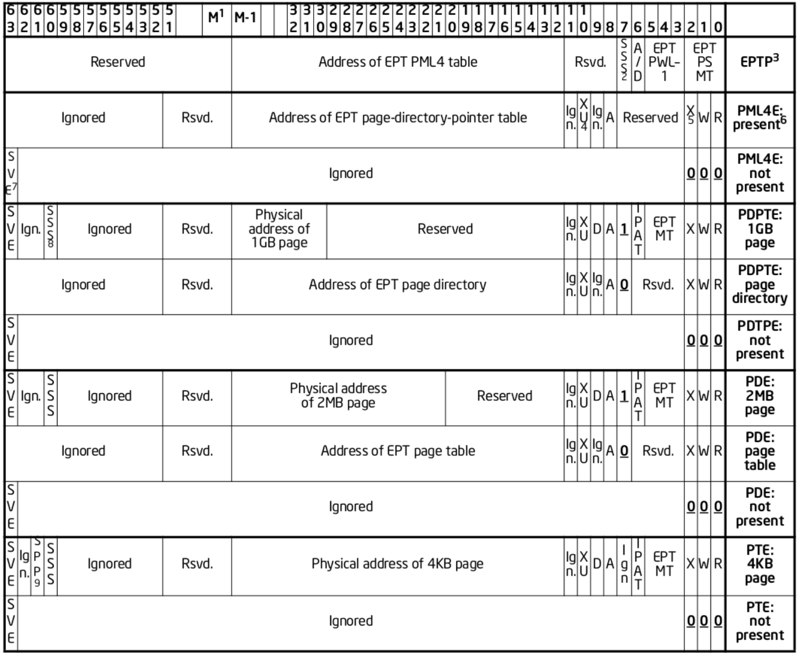
Intel Features

- EPT only used if VM active
- Translations tagged in TLB with EPT base pointer
    - differentiate TLB-entries of different VMs
    - TLB-flush per guest possible
- VPID: virtual processor ID
    - unique value for each VM
    - translations tagged in TLB using VPID



63 62 61 60 59 58 57 56 55 54 53 52 51 M1 M-1 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved | Address of EPT PML4 table | Rsvd. | SSS2 | A/D | EPT PWL-1 | EPT PS MT | EPTP3
Ignored | Rsvd. | Address of EPT page-directory-pointer table | Ign. | XU4 | Ign. | A | Reserved | XS | W | R | PML4E: present6
SVE7 | Ignored | 0 | 0 | 0 | PML4E: not present
SVE | Ign. | SSS8 | Ignored | Rsvd. | Physical address of 1GB page | Reserved | Ign. | XU | D | A | 1 | IPAT | EPT MT | X | W | R | PDPTE: 1GB page
Ignored | Rsvd. | Address of EPT page directory | Ign. | XU | Ign. | A | 0 | Rsvd. | X | W | R | PDPTE: page directory
SVE | Ignored | 0 | 0 | 0 | PDTPE: not present
SVE | Ign. | SSS | Ignored | Rsvd. | Physical address of 2MB page | Reserved | Ign. | XU | D | A | 1 | IPAT | EPT MT | X | W | R | PDE: 2MB page
Ignored | Rsvd. | Address of EPT page table | Ign. | XU | Ign. | A | 0 | Rsvd. | X | W | R | PDE: page table
SVE | Ignored | 0 | 0 | 0 | PDE: not present
SVE | Ign. | SPP9 | SSS | Ignored | Rsvd. | Physical address of 4KB page | Ign. | XU | D | A | Ign | IPAT | EPT MT | X | W | R | PTE: 4KB page
SVE | Ignored | 0 | 0 | 0 | PTE: not present

Figure 28-1. Formats of EPTP and EPT Paging-Structure Entries

Setting up a hypervisor

1. Enable VMX via `CR4`

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2. Allocate a `VMXON` region and use the `VMXON` instruction

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Setting up a hypervisor

1. Enable VMX via `CR4`
2. Allocate a `VMXON` region and use the `VMXON` instruction
3. Allocate an MSR Bitmap region (we don't want a trap for all MSRs)
4. Use `VMCLEAR` instruction

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Virtualization: Trend 2010s → 2022+

Optimization

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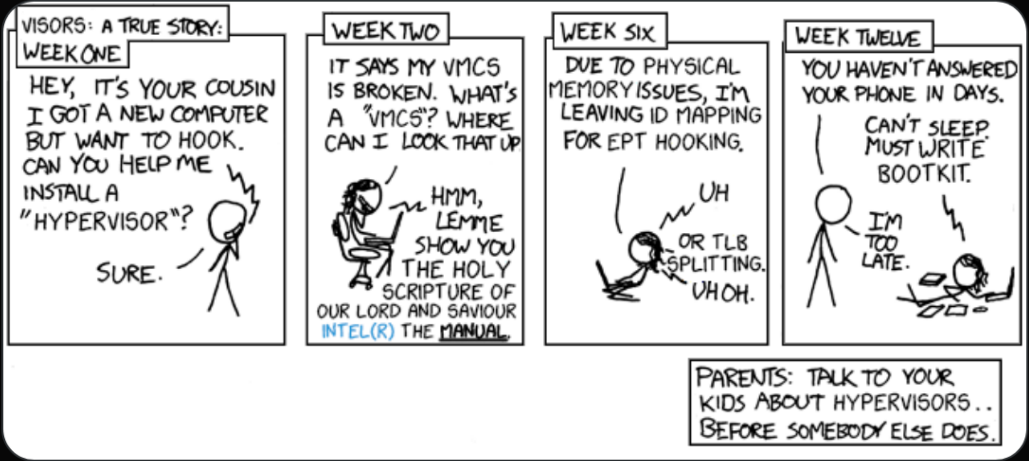
- Context switches between processes are expensive → why not skip process isolation and just use language-level isolation?

This course: hardware-assisted virtualization

Cloud Operating Systems → Hardware-assisted virtualization

cts @gf_256 · 5. Apr. 2020

Talk to your kids about hypervisors...before someone else does


VISORS: A TRUE STORY:
WEEK ONE
HEY, IT'S YOUR COUSIN I GOT A NEW COMPUTER BUT WANT TO HOOK. CAN YOU HELP ME INSTALL A "HYPERVISOR"?
SURE.
WEEK TWO
IT SAYS MY VMCS IS BROKEN. WHAT'S A "VMCS"? WHERE CAN I LOOK THAT UP
HMM, LEMME SHOW YOU THE HOLY SCRIPTURE OF OUR LORD AND SAVIOUR INTEL(R) THE MANUAL.
WEEK SIX
DUE TO PHYSICAL MEMORY ISSUES, I'M LEAVING ID MAPPING FOR EPT HOOKING.
UH
OR TLB SPLITTING.
UH OH.
WEEK TWELVE
YOU HAVEN'T ANSWERED YOUR PHONE IN DAYS.
CAN'T SLEEP MUST WRITE BOOTKIT.
I'M TOO LATE.
PARENTS: TALK TO YOUR KIDS ABOUT HYPERVISORS.. BEFORE SOMEBODY ELSE DOES.

19 60

CloudOS: the third time

- Seminar-style

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- Seminar-style
- You code

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- You present

Team

Daniel Gruss, Andreas Kogler, Fabian Rauscher, Sudheendra Neela

Grading Scale

- 100 P. $=$ 100%

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Teams

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→ send us your registration until Friday March 10

Teams

- Deadlines: Friday 23:59

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- Grace Period: 48 hours **but no support**

Timeline & Deadlines

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  Estimated Team Effort: 125h, Points: 5P.

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- 16.6. Successful Live Presentation at 21:00, Bonus Points: 5P.