Cloud Operating Systems

Booting x86

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2022-03-21

Real Mode

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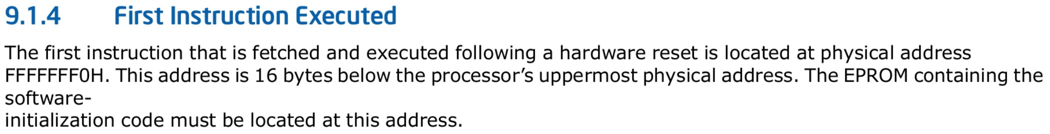
- Direct physical memory access

Booting x86 Intel



9.1.4 First Instruction Executed

The first instruction that is fetched and executed following a hardware reset is located at physical address FFFFFFF0H. This address is 16 bytes below the processor’s uppermost physical address. The EPROM containing the software-
initialization code must be located at this address.

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    - physical address space $\neq$ RAM directly mapped

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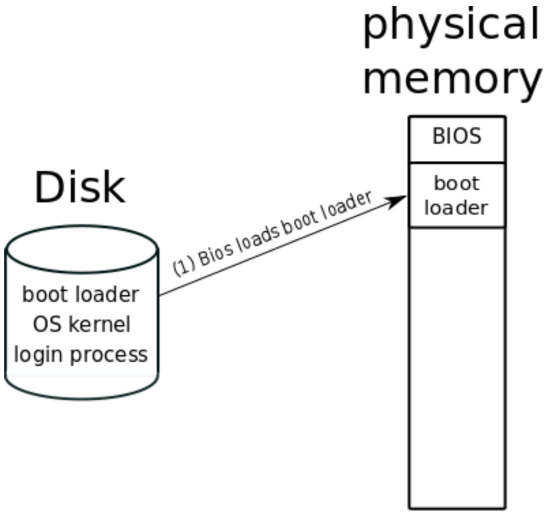
- Execute code from the MBR
- MBR code usually loads more data from the disk into memory

Booting x86 Intel (Illustration)



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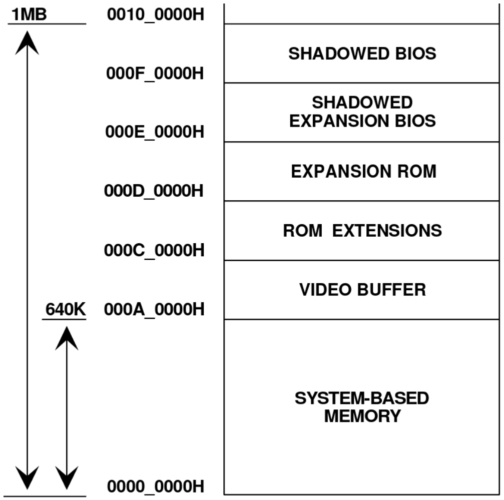
→ BIOS calls!

- We can trigger standardized software interrupts and let the BIOS handle it!

Real Mode - Memory Layout



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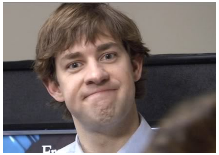

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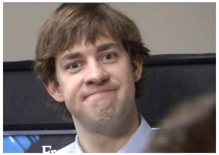

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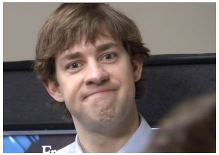

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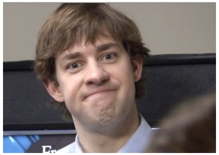

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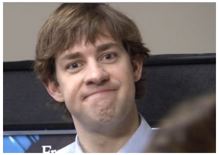

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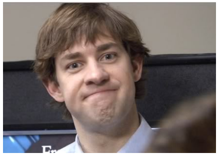

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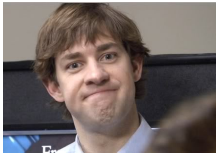

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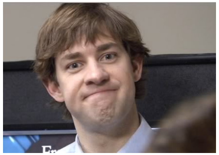

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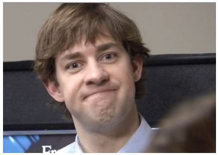

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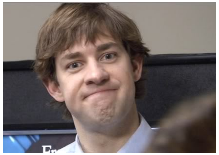

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- Load DS, ES, FS, GS, SS, ESP

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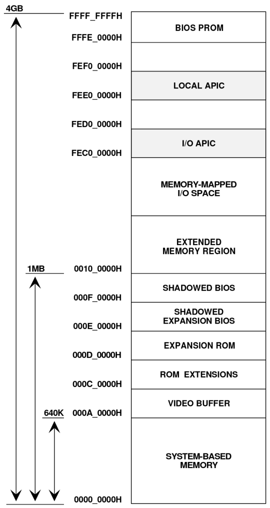
- Optional paging

Protected Mode - Memory Layout



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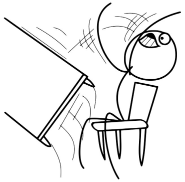

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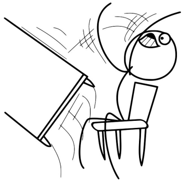

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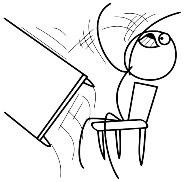

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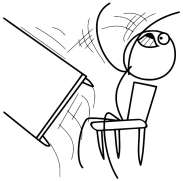

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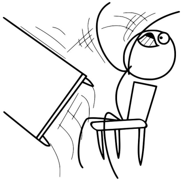

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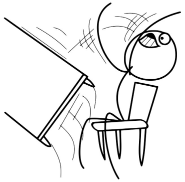

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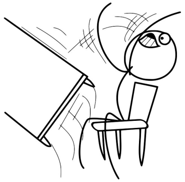

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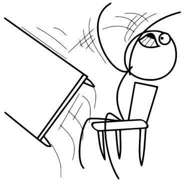

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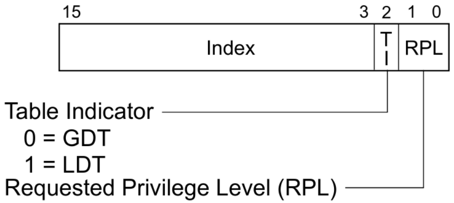
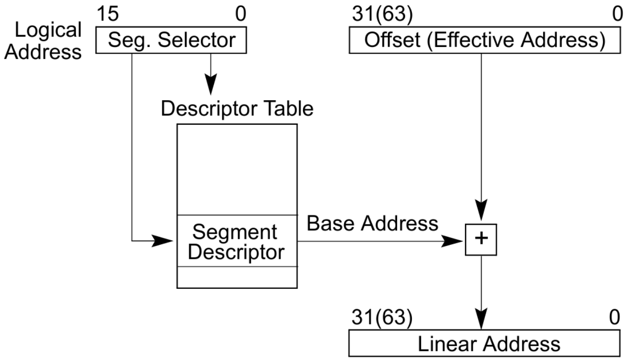
    - Flags

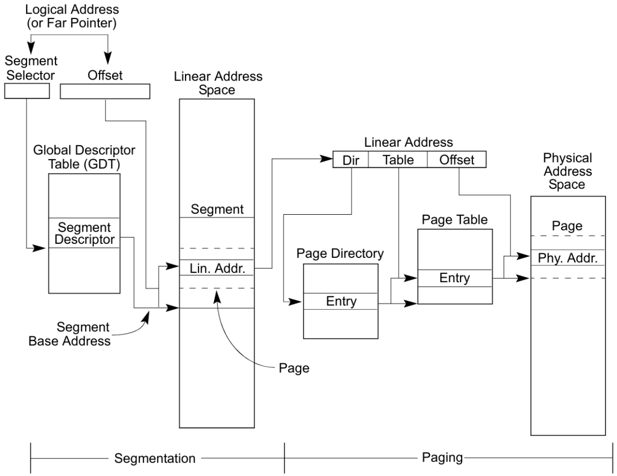
Segment Register



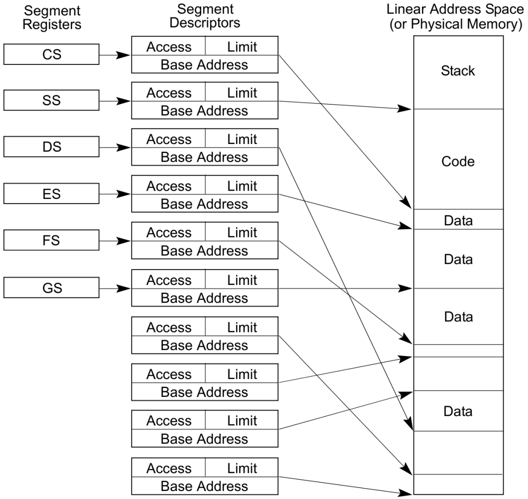
Segmentation Inner Workings



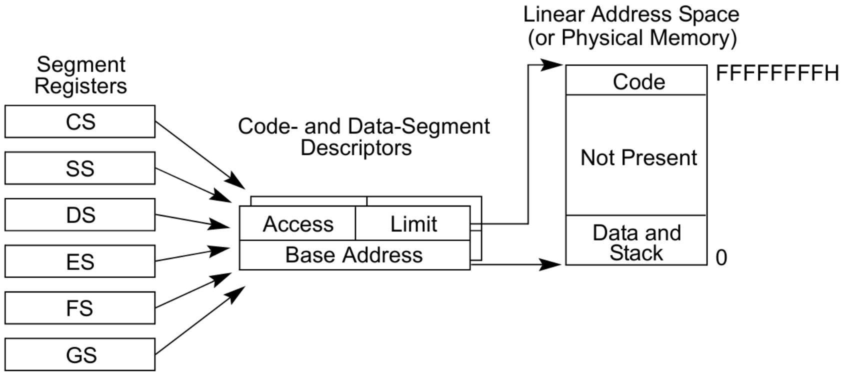
Segmentation with Paging



Segmentation Dream



Segmentation Reality



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- Reload segment selectors to enter long mode proper

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Booting SWEB

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