ARMageddon

How Your Smartphone CPU Breaks Software-Level Security And Privacy

Moritz Lipp and Clémentine Maurice

November 3, 2016—Black Hat Europe

Motivation

- Safe software infrastructure does not mean safe execution

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Motivation

- Safe software infrastructure does not mean safe execution
- Information leaks because of the underlying hardware
- We focus on the CPU cache
- Cache attacks can be used for covert communications and attack crypto implementations
- Only been demonstrated on Intel x86 for now
- But why not on ARM?

Who We Are

Who We Are

- **Moritz Lipp**
- Master Student, Graz University Of Technology
- 🐦 @mlqxyz
- ✉ mail@mlq.me

Who We Are

- **Clémentine Maurice**
- PhD in InfoSec; Postdoc, Graz University Of Technology
- 🐦 @BloodyTangerine
- ✉ clementine.maurice@iaik.tugraz.at

The rest of the team

The rest of the research team

- Daniel Gruss
- Raphael Spreitzer
- Stefan Mangard

From Graz University of Technology

Demo

Outline

- Background information

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- What are the challenges for cache attacks on ARM?

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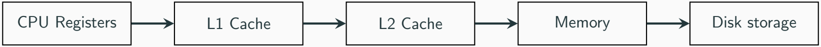
- What are the challenges for cache attacks on ARM?
- How to solve those challenges
- Attack scenarios
- Tools

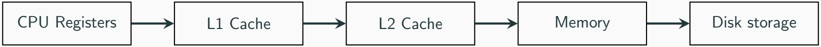
Cache Attacks

Memory Hierarchy



- Data can reside in

Memory Hierarchy



- Data can reside in
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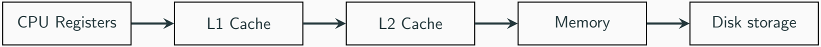

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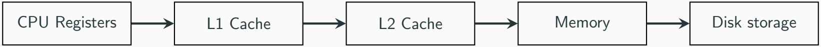

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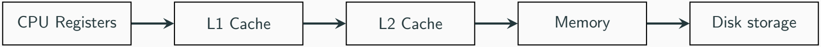

- Data can reside in
    - CPU registers
    - Different levels of the CPU cache
    - Main memory
    - Disk storage

Cache Attacks

- Exploit timing differences of memory accesses:

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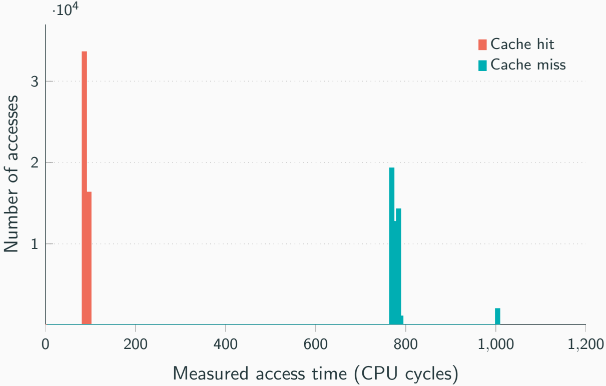
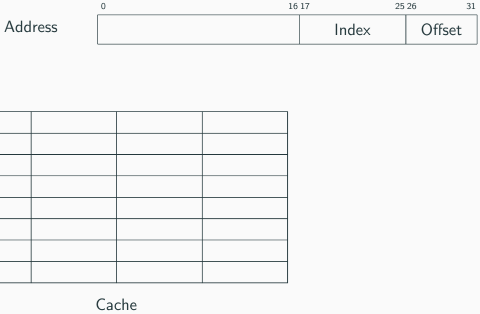


Set-Associative Caches



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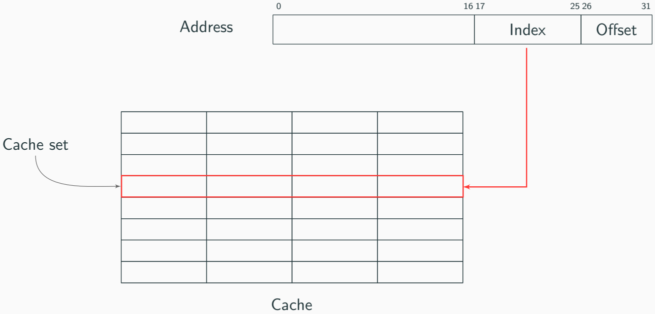

Data loaded in a specific set depending on its address

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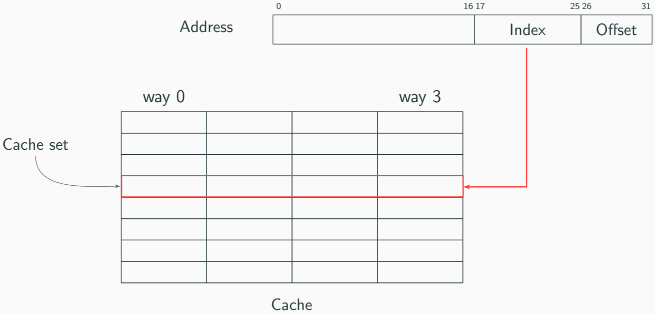

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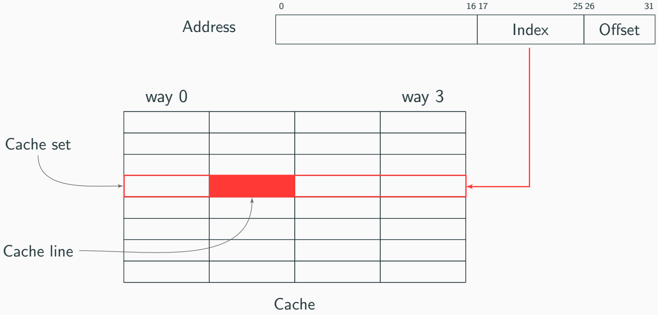
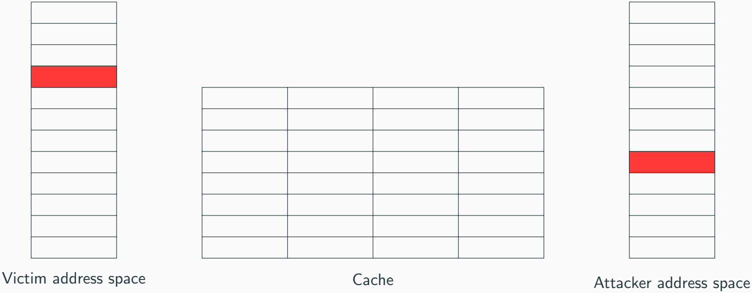


Data loaded in a specific set depending on its address

Several ways per set

Cache line loaded in a specific way depending on the replacement policy

Cache Attacks: Flush+Reload



Step 1: Attacker maps shared library (shared memory, in cache)

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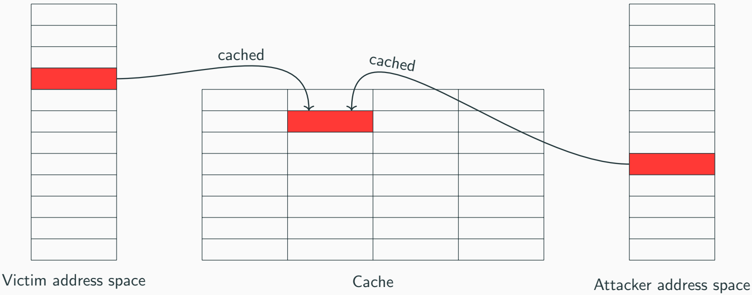

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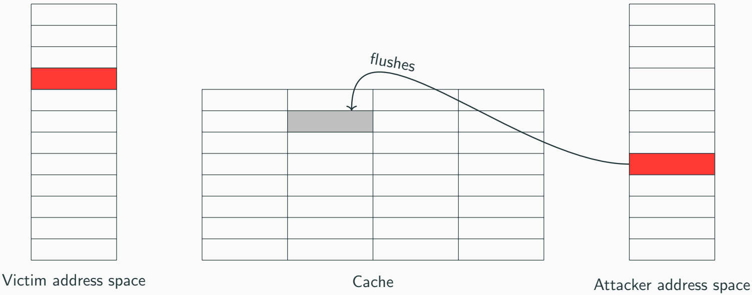

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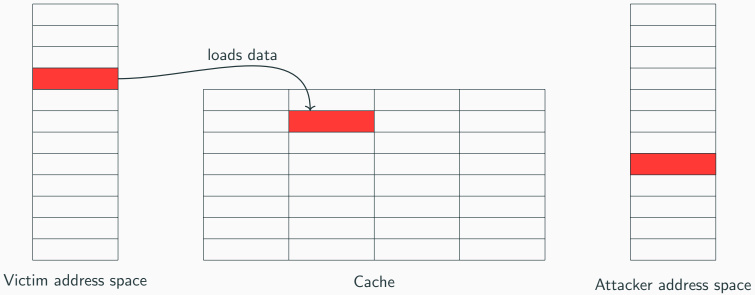

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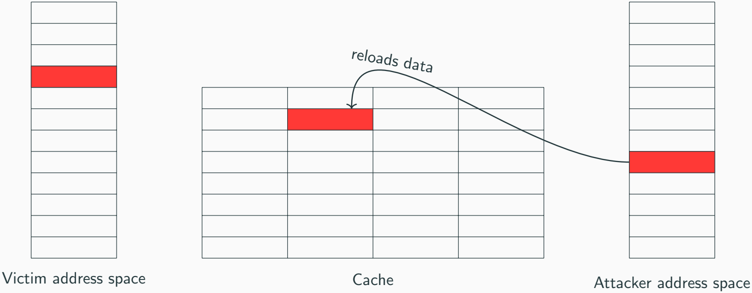

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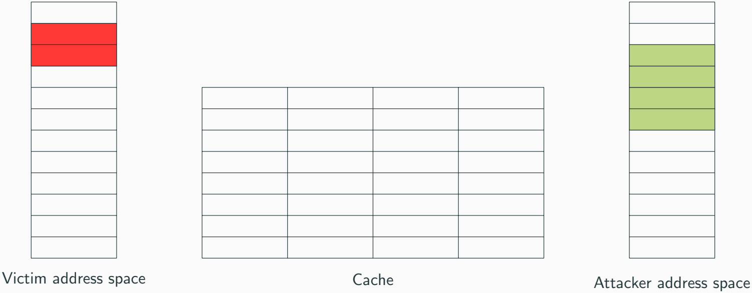
Step 4: Attacker reloads the data

Cache Attacks: Prime+Probe



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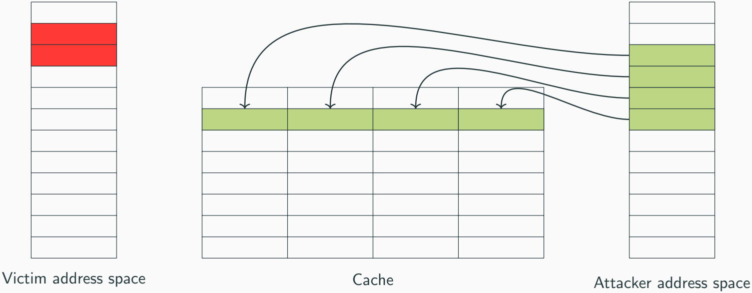

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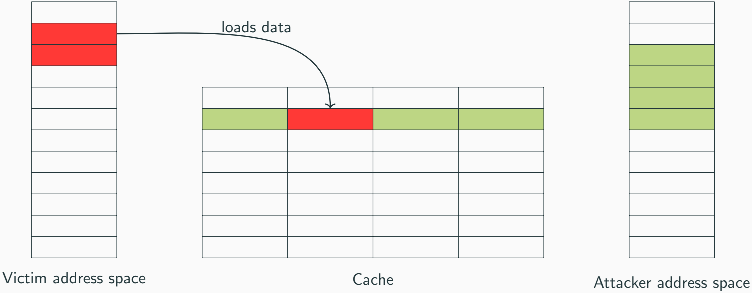

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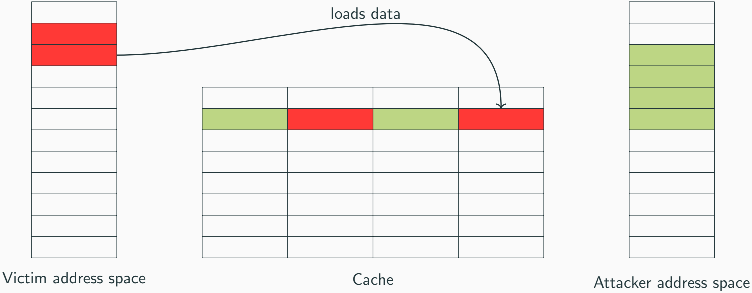

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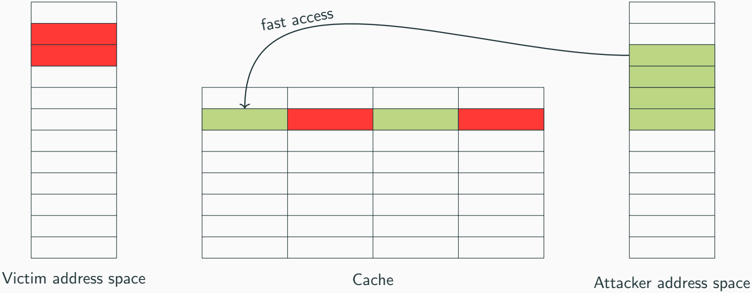

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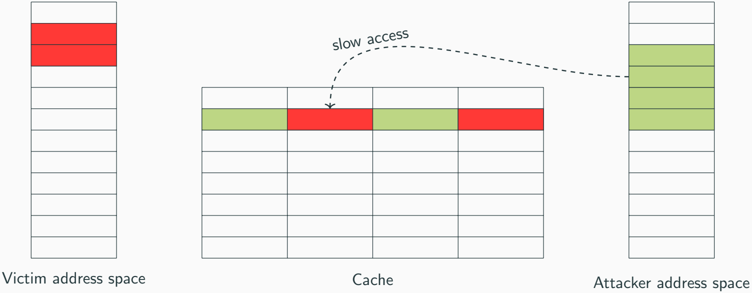

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Differences between Intel x86 and ARM

Cache maintenance

- Basic operation for cache attacks: invalidate cache lines

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  - Intel x86: Unprivileged `clflush` instruction
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Challenge #1

No flush instruction

Cache eviction

- Fill the whole cache

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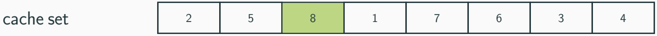

cache set	2	5	8	1	7	6	3	4

Cache eviction

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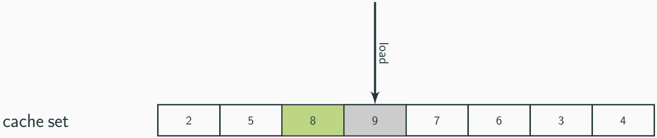

load

cache set	2	5	8	9	7	6	3	4

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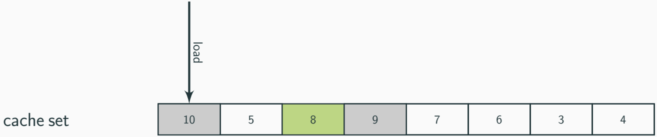

load

cache set	10	5	8	9	7	6	3	4

Cache eviction

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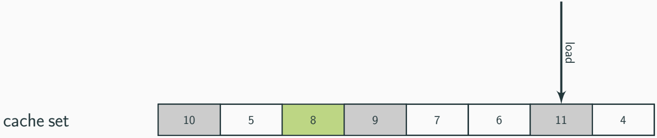

load

cache set	10	5	8	9	7	6	11	4

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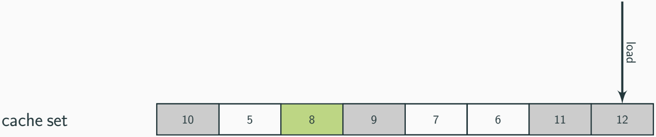

load

cache set	10	5	8	9	7	6	11	12

Cache eviction

- Fill the whole cache → too slow
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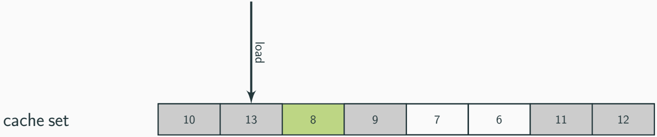

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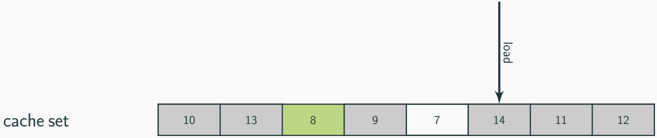

load

cache set	10	13	8	9	7	14	11	12

Cache eviction

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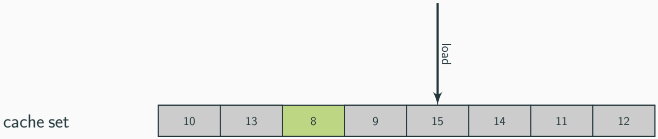

Cache eviction

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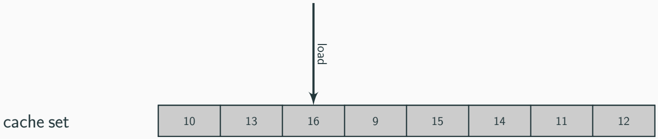
- Until the target address is evicted from the cache



load

cache set

10	13	16	9	15	14	11	12

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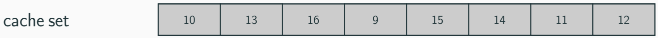

cache set	10	13	16	9	15	14	11	12

→ Ideal case with LRU replacement policy

Cache eviction (what actually happens)

- Pseudo-random cache replacement policy

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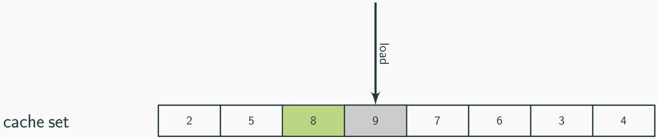

load

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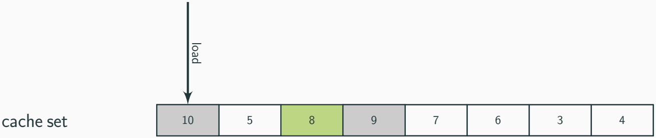

load

cache set

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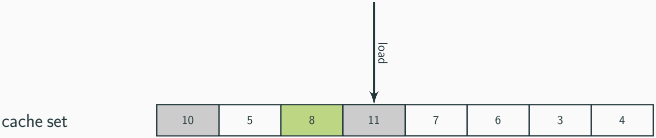

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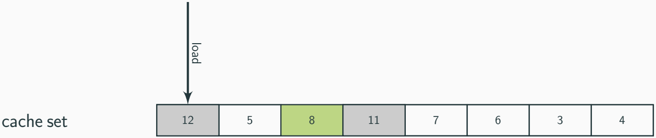

load

cache set	12	5	8	11	7	6	3	4

Cache eviction (what actually happens)

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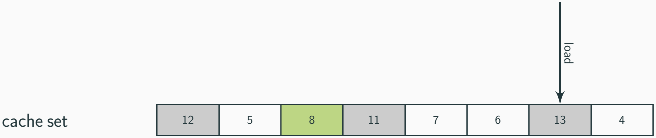

load

cache set								
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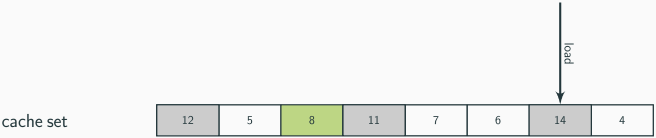

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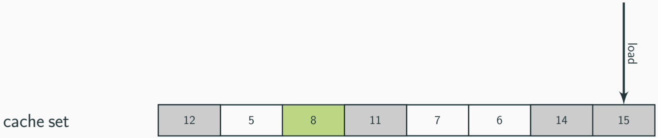

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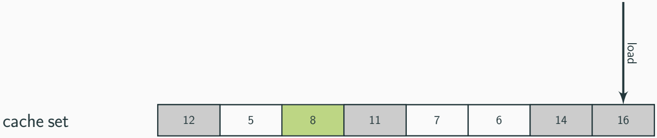

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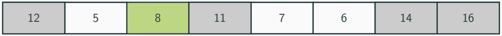

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→ Simple approach highly inefficient

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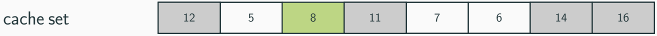

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Challenge #2

Pseudo-random replacement policy complicates eviction

Timing measurements

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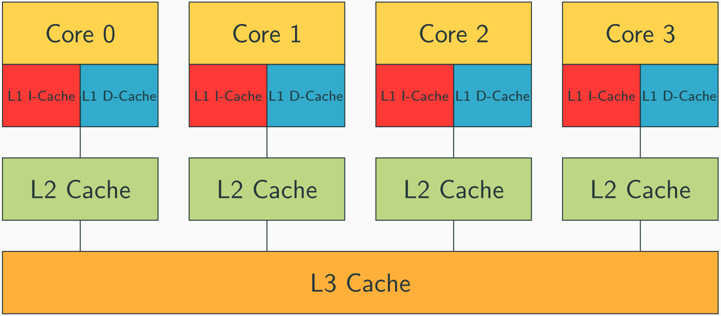
Challenge #3

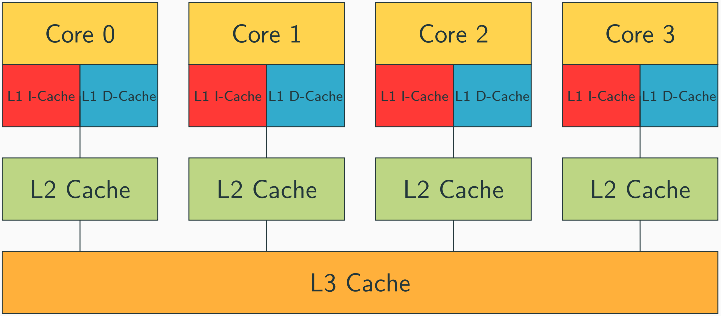
No unprivileged and accurate timing sources

Cache Hierarchy on Intel CPUs



- Last-level cache: L3

Cache Hierarchy on Intel CPUs



- Last-level cache: L3
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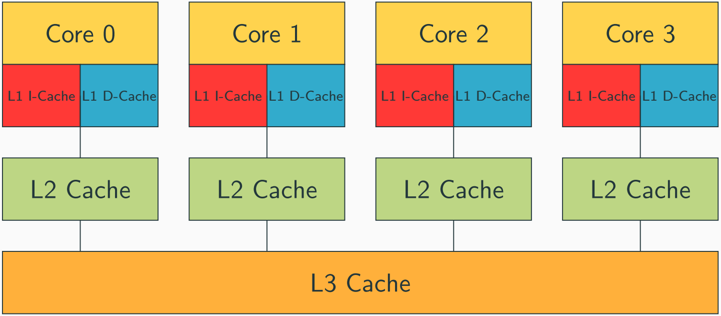

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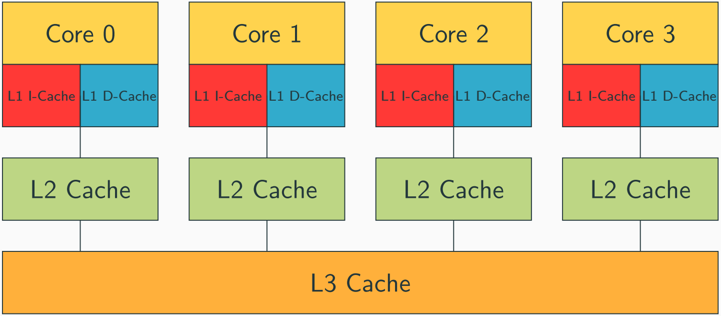

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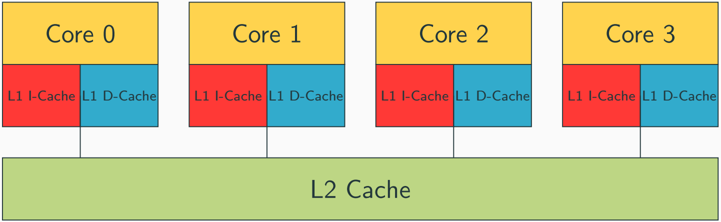
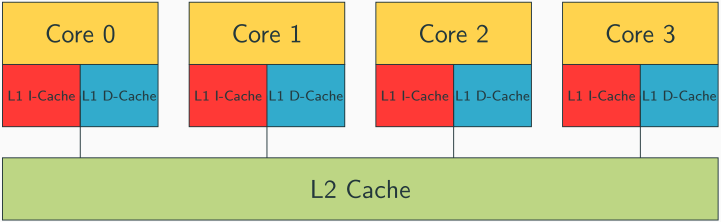
  → Shared memory is shared in the cache across all cores

Cache Hierarchy on ARM Cortex-A CPUs



- Last-level cache: L2

Cache Hierarchy on ARM Cortex-A CPUs



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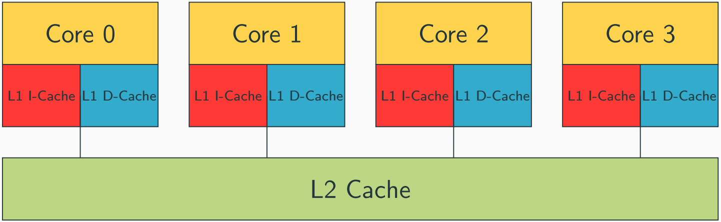
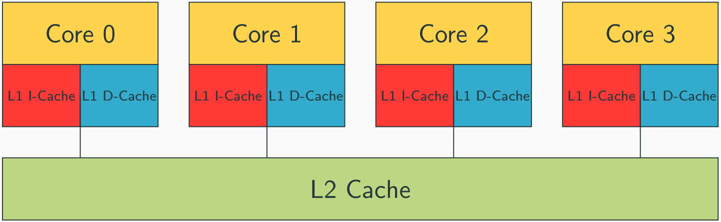


- Last-level cache: L2
  - **shared**
  - not **inclusive**

Cache Hierarchy on ARM Cortex-A CPUs



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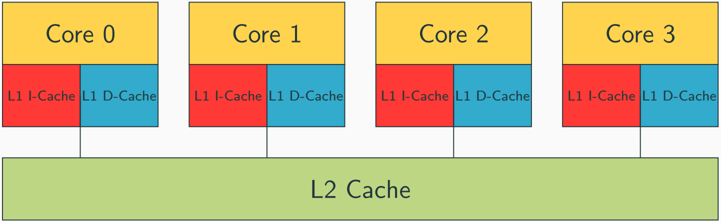

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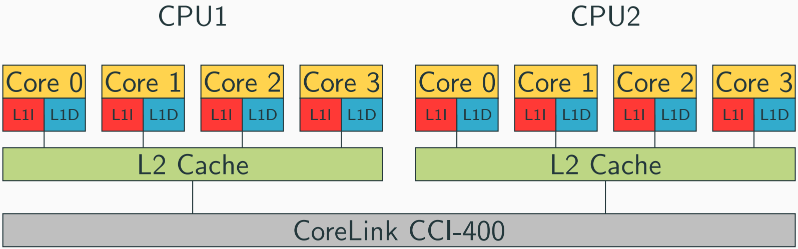
Challenge #4

Non-inclusive caches

Cache Hierarchy on ARM big.LITTLE



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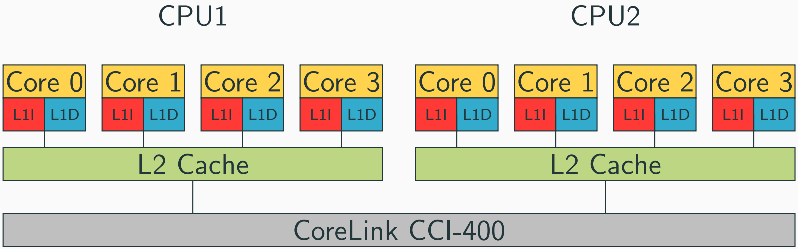
Cache Hierarchy on ARM big.LITTLE



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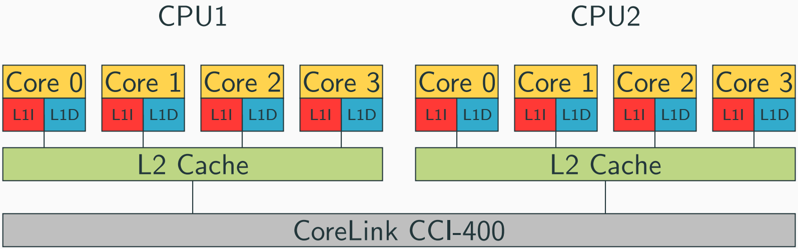

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Challenge #5

No shared cache

Let’s solve those challenges

Challenges

Challenge #1 No flush instruction

Challenge #2 Pseudo-random replacement policy

Challenge #3 No unprivileged timing

Challenge #4 Non-inclusive caches

Challenge #5 No shared cache

Solving #1: No flush instruction

- Replace the missing flush instruction with cache eviction

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Solving #1: No flush instruction

- Replace the missing flush instruction with cache eviction
- Works on Intel x86
  - *Prime+Probe*
  - *Flush+Reload* → *Evict+Reload*

Challenges

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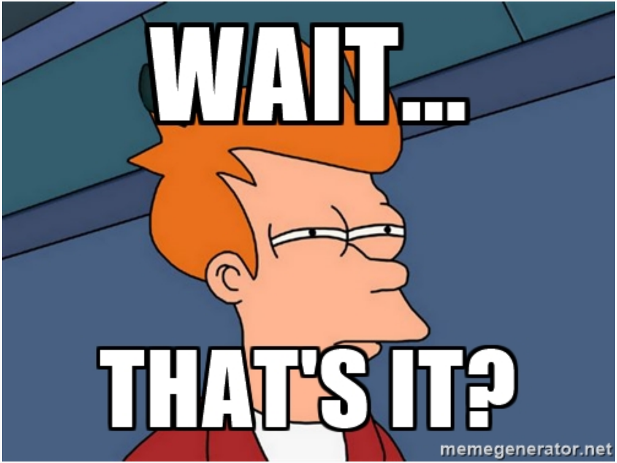
Challenges



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→ Central idea of our Rowhammer.js paper

Solving #2: Pseudo-random replacement policy

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- Accessing once *n* addresses in an *n*-way cache set

  → Cache eviction slow and unreliable

Solution:

- Accessing unique addresses several times, with different access patterns

Solving #2: Pseudo-random replacement policy

Table 1: Different eviction strategies for the Alcatel One Touch Pop 2

Addresses	Accesses	Cycles	Eviction rate
48	48	6 517 ✓	70.78% ✗

Solving #2: Pseudo-random replacement policy

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Solving #2: Pseudo-random replacement policy

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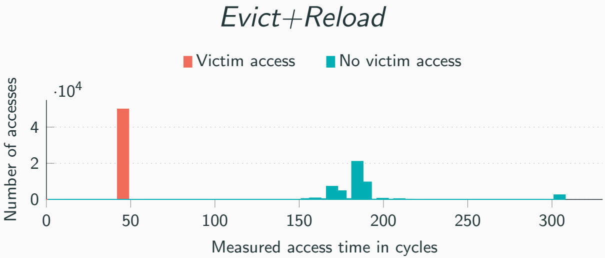
  - Execute on target device
  - Evaluate log files and build result database
- Find fast and efficient eviction strategies for any device

Solving #2: Pseudo-random replacement policy



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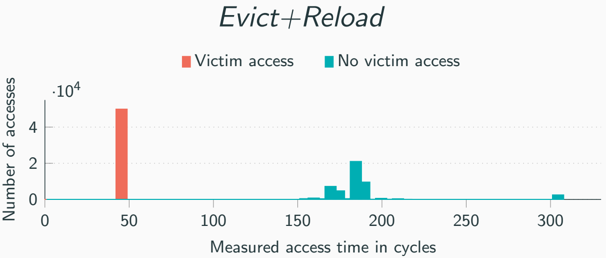

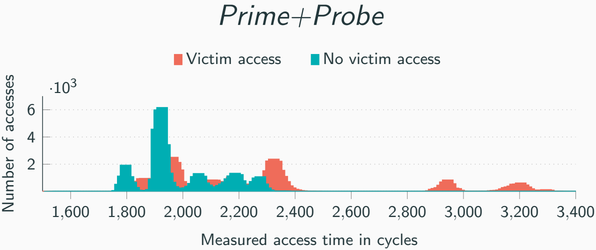

Challenges

Challenge #1 No flush instruction ✔

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Challenge #3 No unprivileged timing

Challenge #4 Non-inclusive caches

Challenge #5 No shared cache

Solving #3: No unprivileged timing

1. Performance counter: Privileged

Solving #3: No unprivileged timing

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→ Allows distinguishing cache hits from cache misses

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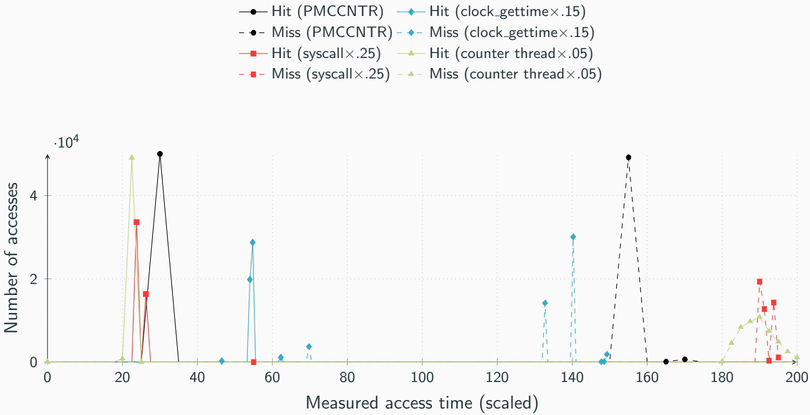

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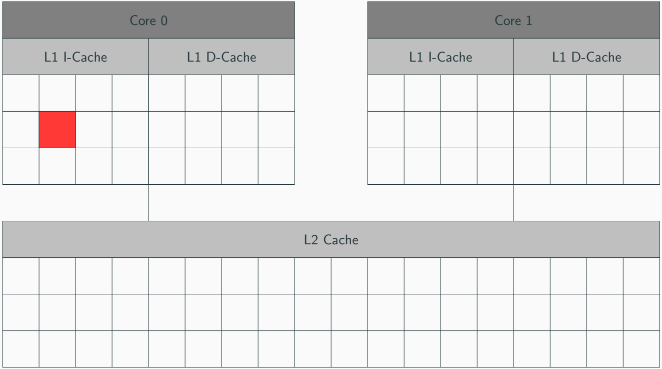

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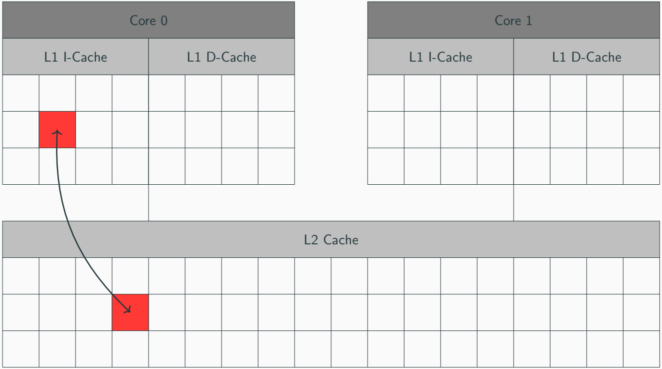

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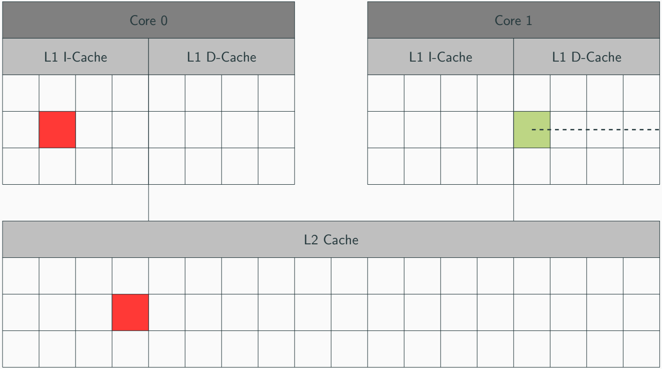

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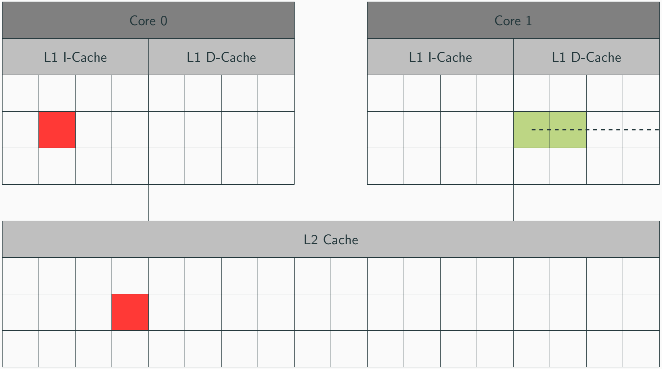

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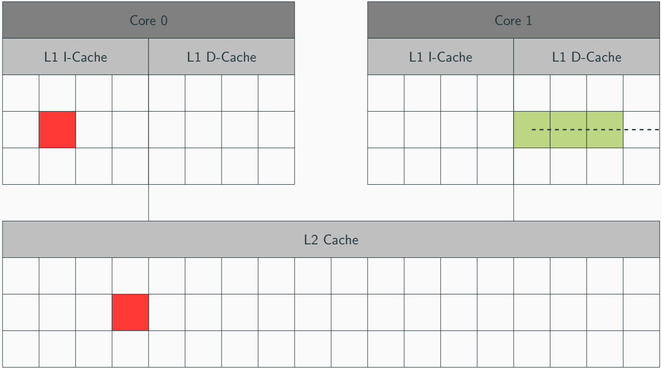

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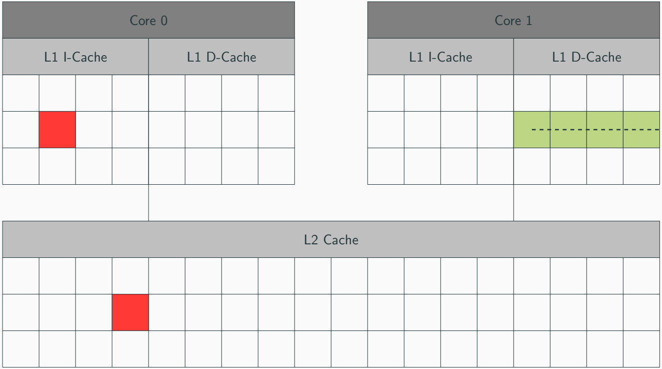

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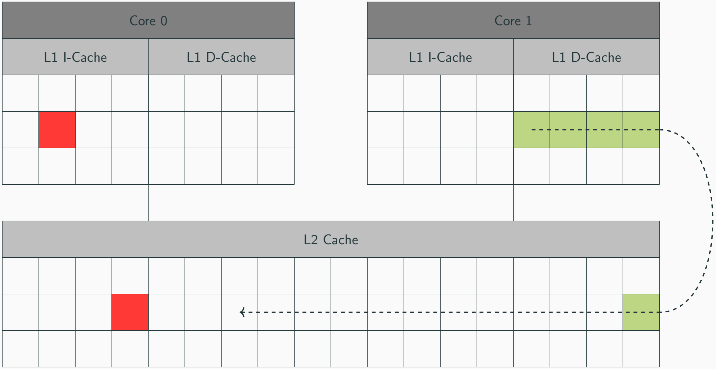

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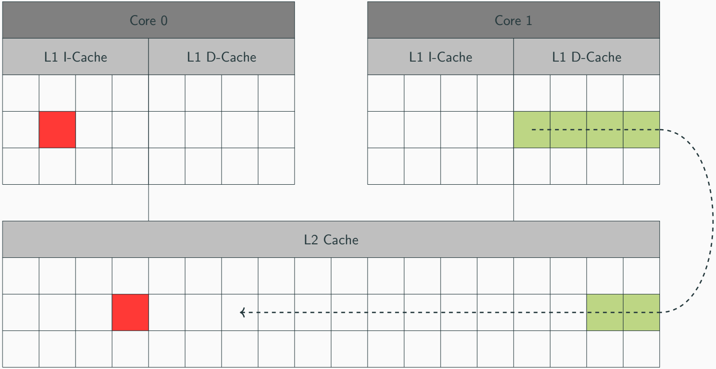

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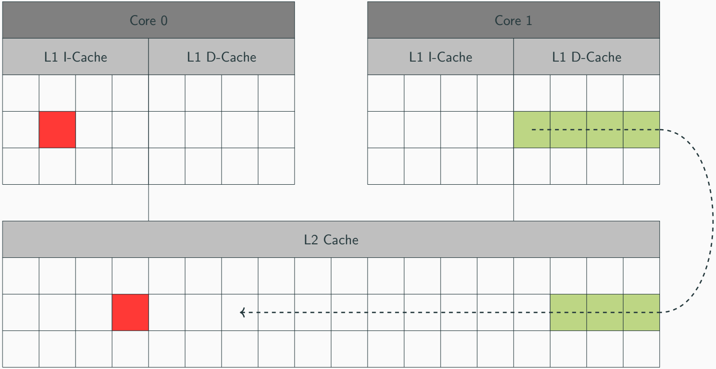

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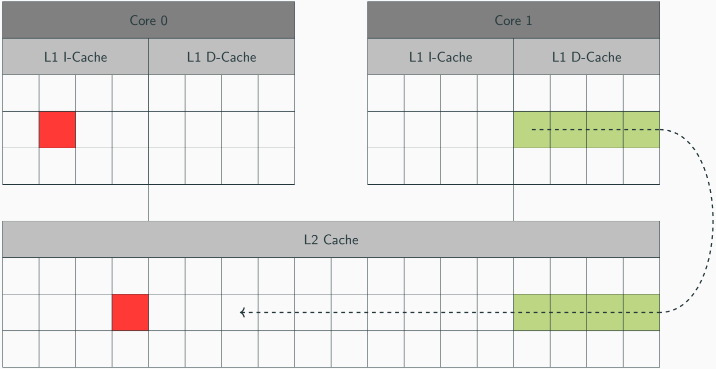

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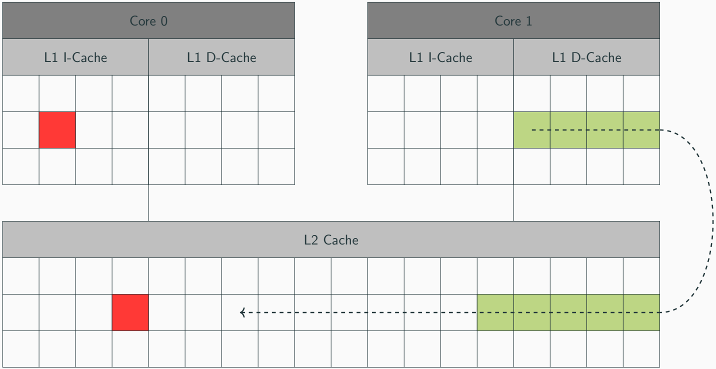

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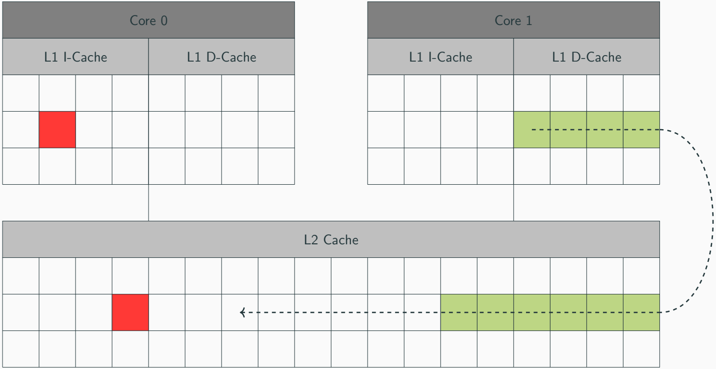

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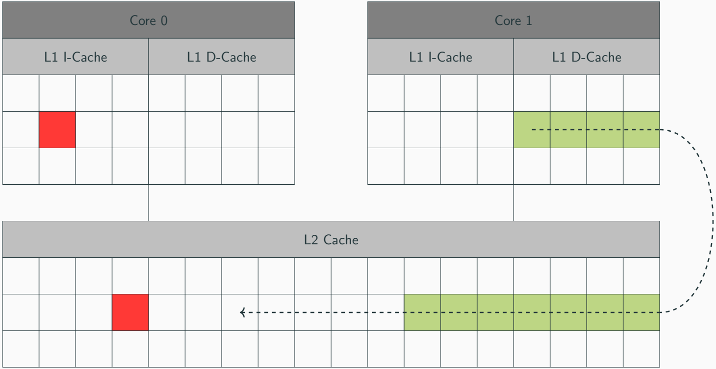

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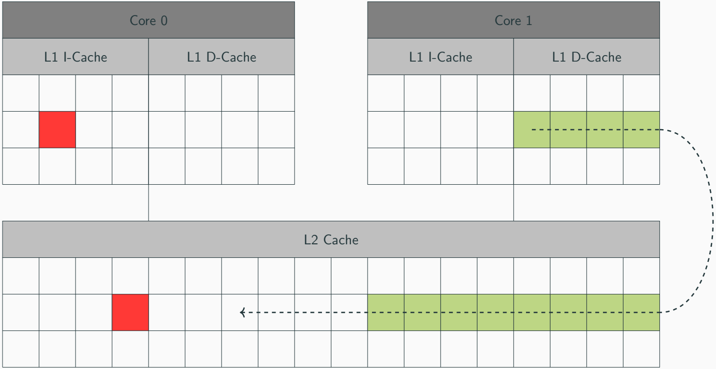

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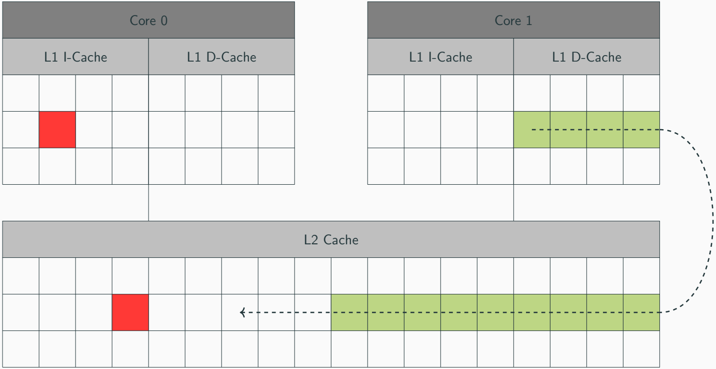

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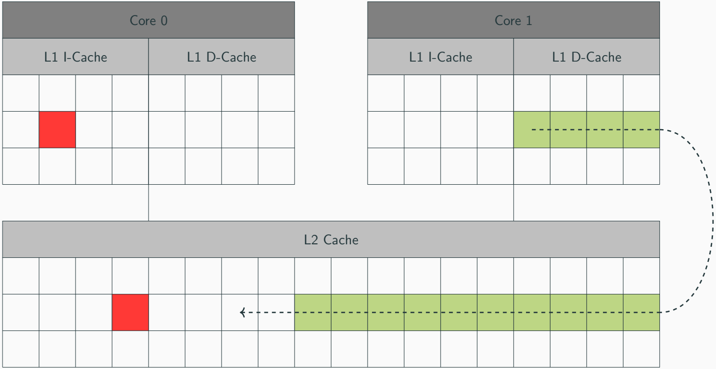

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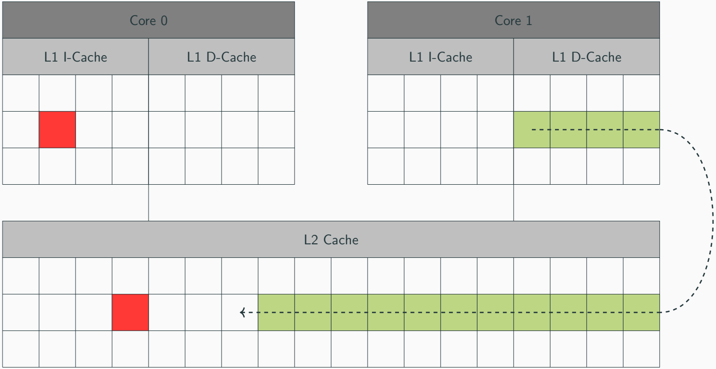

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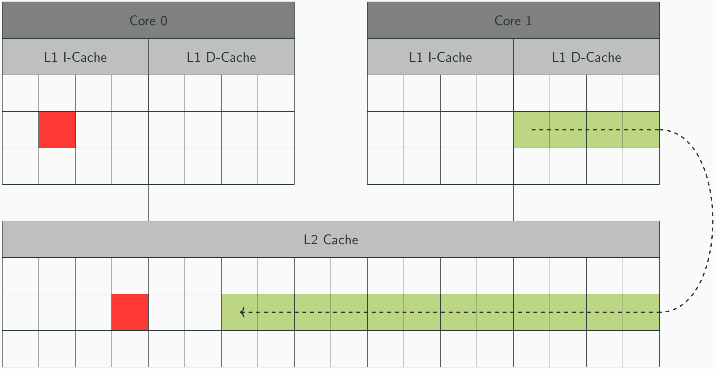

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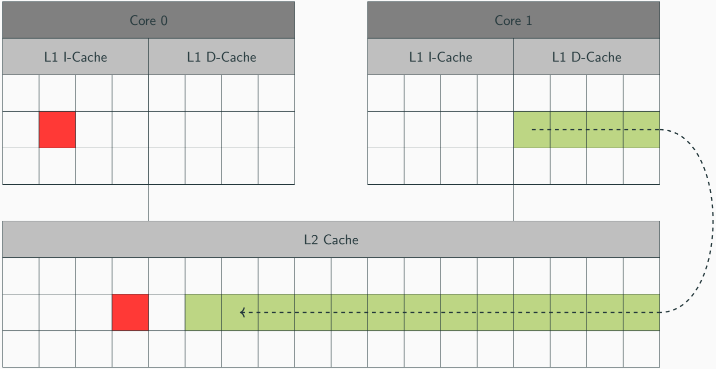

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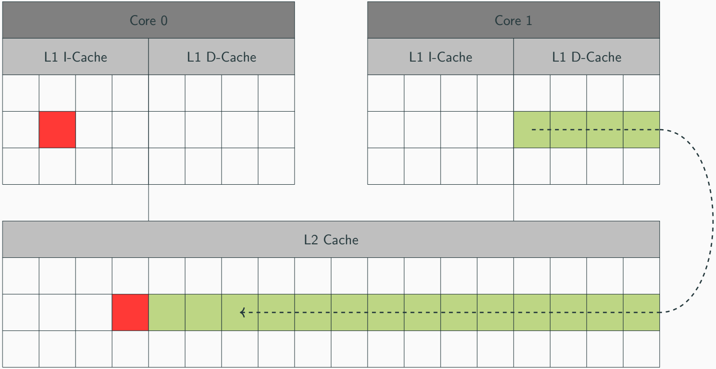

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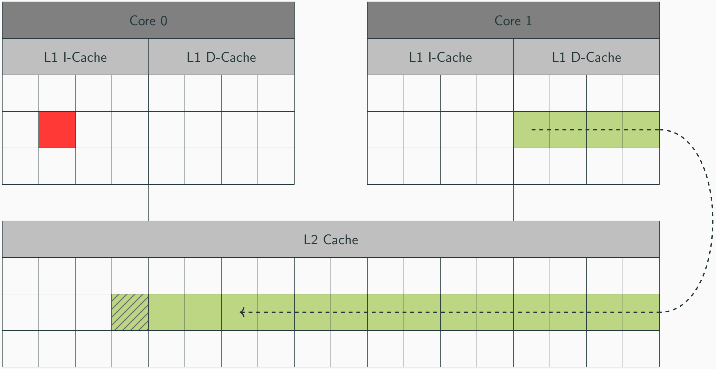

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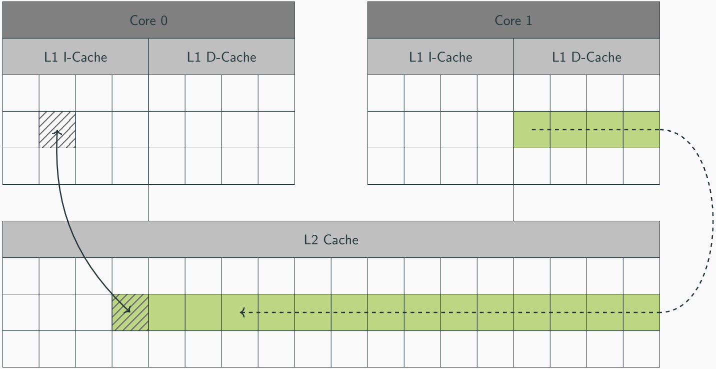

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Solving #4: Non-inclusive caches

- How can we determine if the victim has loaded the address?
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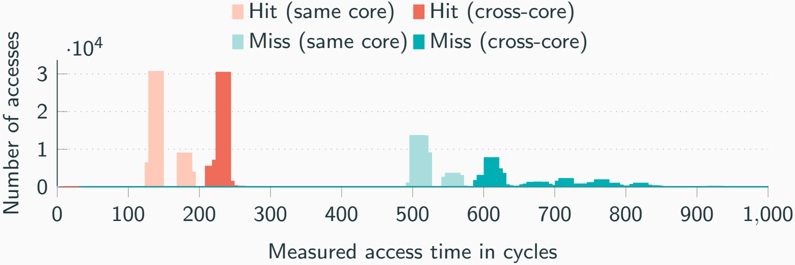
→ Detect if another core has accessed the memory location



Challenges

Challenge #1 No flush instruction ✔

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Challenge #3 No unprivileged timing ✔

Challenge #4 Non-inclusive caches ✔

Challenge #5 No shared cache

Solving #5: No shared cache

- Multiple CPUs that do not share a cache

Solving #5: No shared cache

- Multiple CPUs that do not share a cache
- Cache coherency protocol (again)

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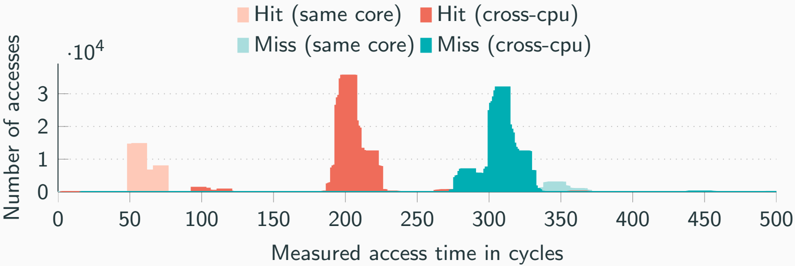

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Attack scenarios

Case study #1

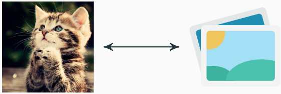
Covert communication

Case Study #1: Covert Channel

- Malicious privacy gallery app

Case Study #1: Covert Channel

- Malicious privacy gallery app
  - No permissions except accessing your images



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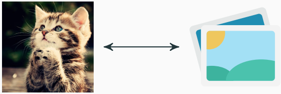

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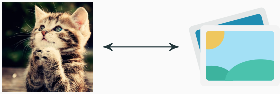

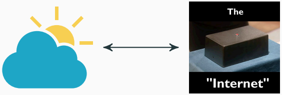

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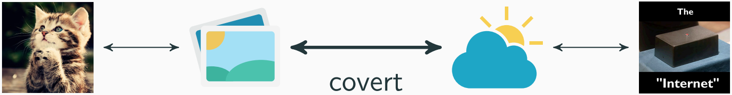

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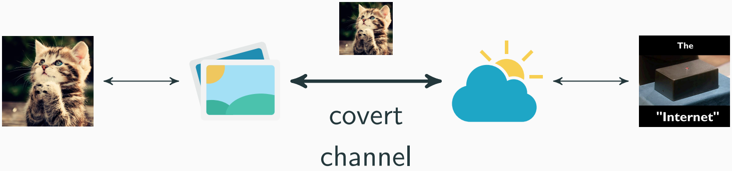
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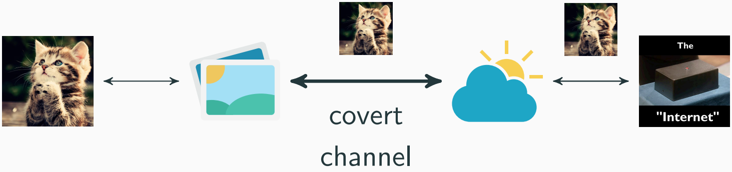

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  - Use a sequence number (SQN)
  - Protect payload and sequence number with a checksum

31 24	23 8	7 0
Sender SQN	Payload	CRC

10 3	2 0
Receiver SQN	CRC

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Ours (OnePlus One)	*Evict+Reload*, cross-core	12 537	5.00%
Ours (Alcatel One Touch Pop 2)	*Evict+Reload*, cross-core	13 618	3.79%
Ours (Samsung Galaxy S6)	*Flush+Flush*, cross-core	178 292	0.48%
Ours (Samsung Galaxy S6)	*Flush+Reload*, cross-CPU	257 509	1.83%
Ours (Samsung Galaxy S6)	*Flush+Reload*, cross-core	1 140 650	1.10%

Case study #2

Spying on the user

Case Study #2: Spying on the User

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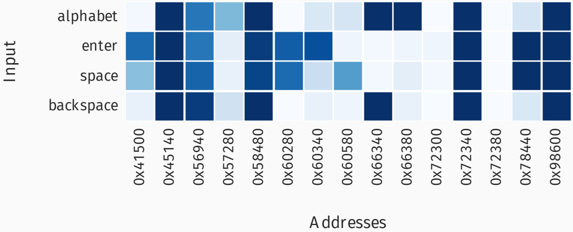

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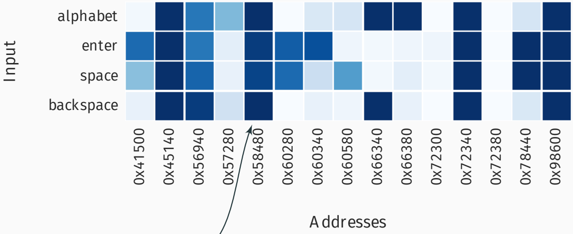

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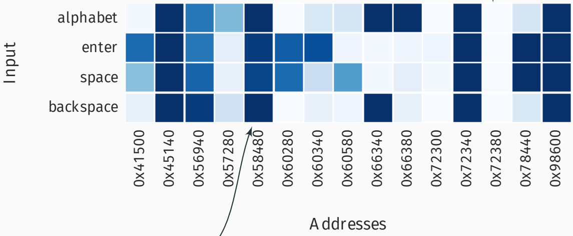

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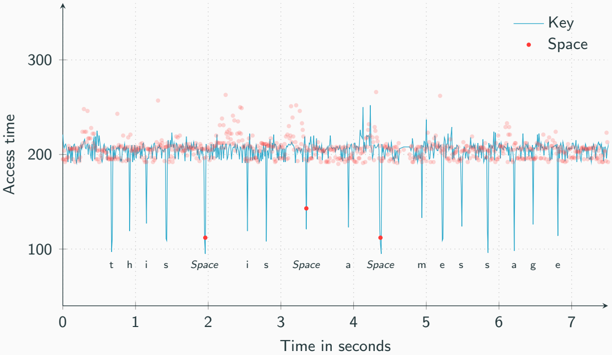
Evict+Reload on two addresses on the Alcatel One Touch Pop 2 in `custpack@app@withoutlibs@LatinIME.apk@classes.dex`
→ Differentiate keys from spaces



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→ Recovering accessed table indices ⇒ recovering the key

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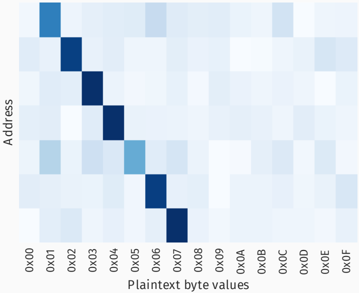

Case study #4

Monitoring ARM TrustZone

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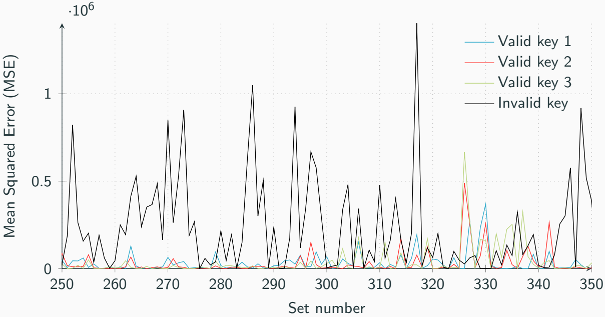

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ARMageddon

How Your Smartphone CPU Breaks Software-Level Security And Privacy

Moritz Lipp and Clémentine Maurice

November 3, 2016—Black Hat Europe