

Searching traps in Zilog Z80 CPU

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The presented method allows distinguishing of depleted transistors from normal transistors. For that the Z80 sample was decapsulated and deprocessed layer by layer down to substrate transistor layer. For reference, the image of the die with metal layer removed is presented in Figure 1. This image still contains the imprinting of metal wires in the interlayer oxide making it possible to trace all the connections from single image.

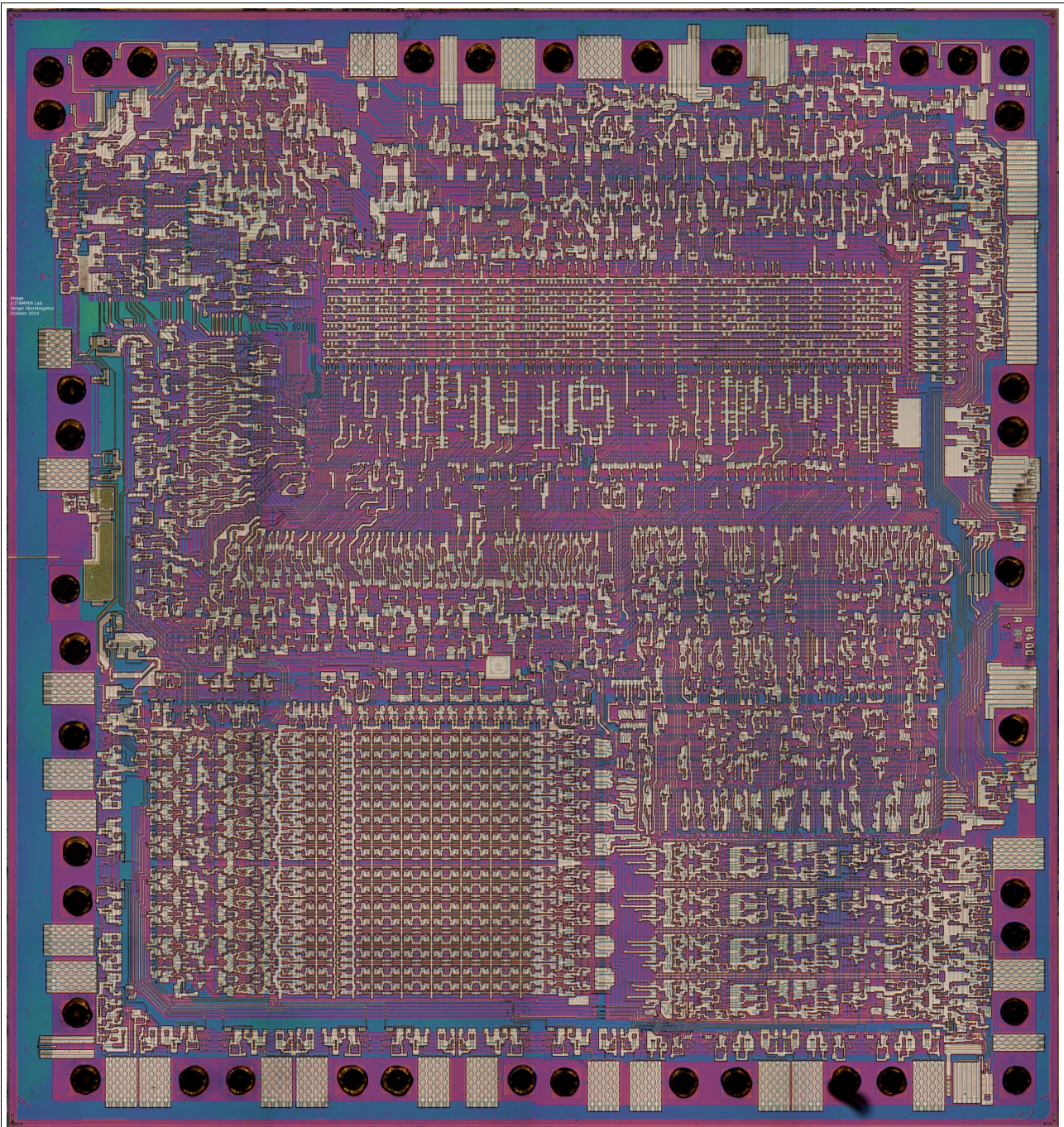


Fig.2. Brightfield image with 10x objective of the GoldStar Z80 die after the metal was removed.

Finally a doping selective etching was used to make depleted transistors visible. They are better to

observe with darkfield illumination which make edges between the doping and substrate well visible (Figure 2).

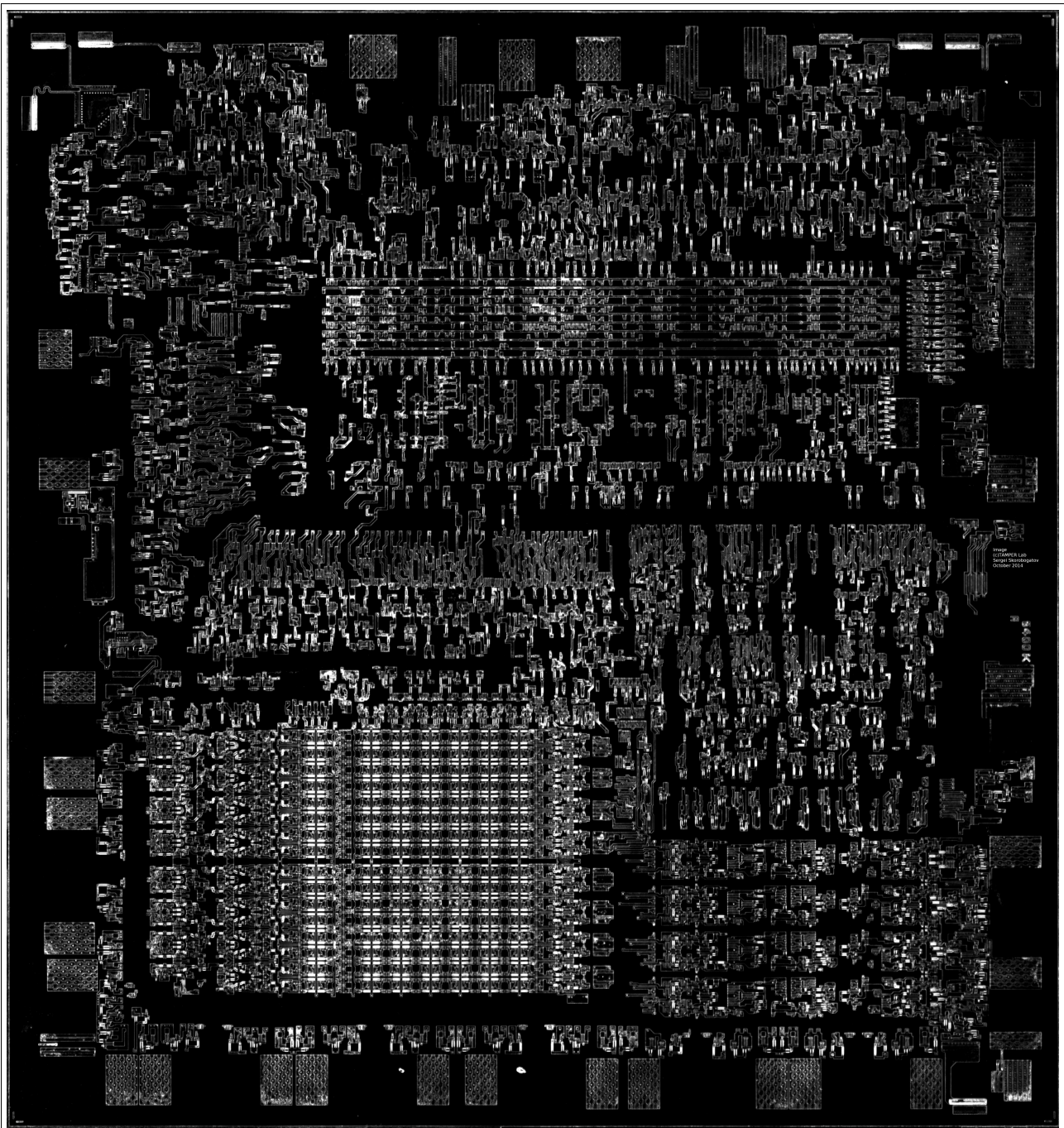


Fig.2. Darkfield image with 10x objective of the Zilog Z80 die after treatment.

Five suspected candidates for trap transistors were investigated. The images of the relevant areas under higher magnification are presented with brightfield and darkfield illuminations. First transistor is located in the top left corner (Figure 3). Both brightfield and darkfield images show similarity of one of the transistors with depleted transistors (large ones). The edge on the transistor's side adjacent to the substrate is darker in the brightfield image and illuminated in the brightfield image. Second transistor is located below the first one (Figure 4). Third transistor is in the top right corner (Figure 5). Fourth transistor is in the centre of the die (Figure 6). The suspected fifth transistor located in the middle left is not a trap one as it looks the same as normal transistors (Figure 7).

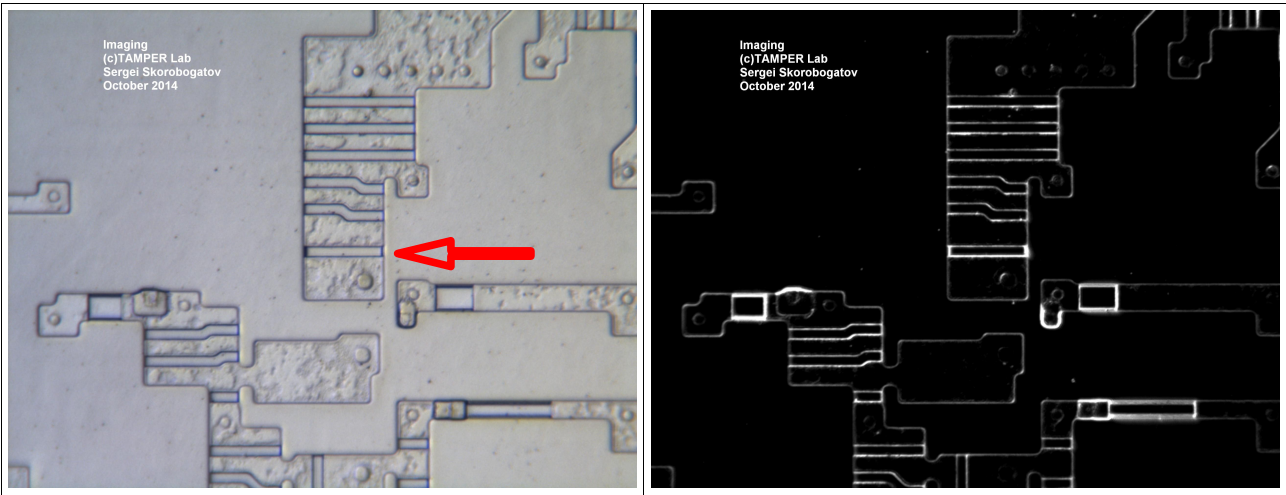


Fig.3. Brightfield and darkfield images with 50x objective of the transistor 1 area (top left corner, top transistor).

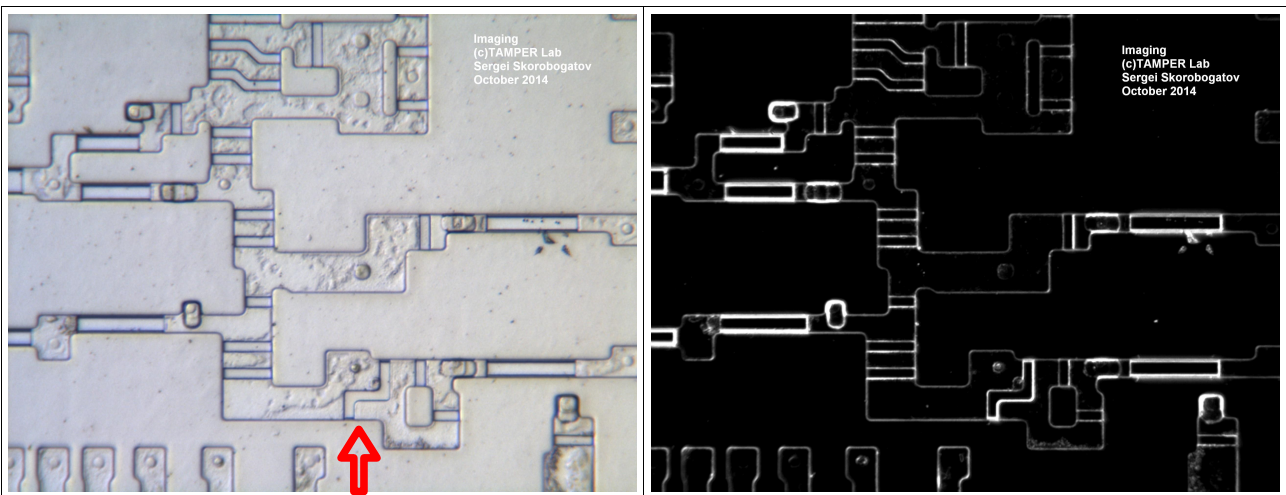


Fig.4. Brightfield and darkfield images with 50x objective of the transistor 2 area (top left corner, bottom transistor).

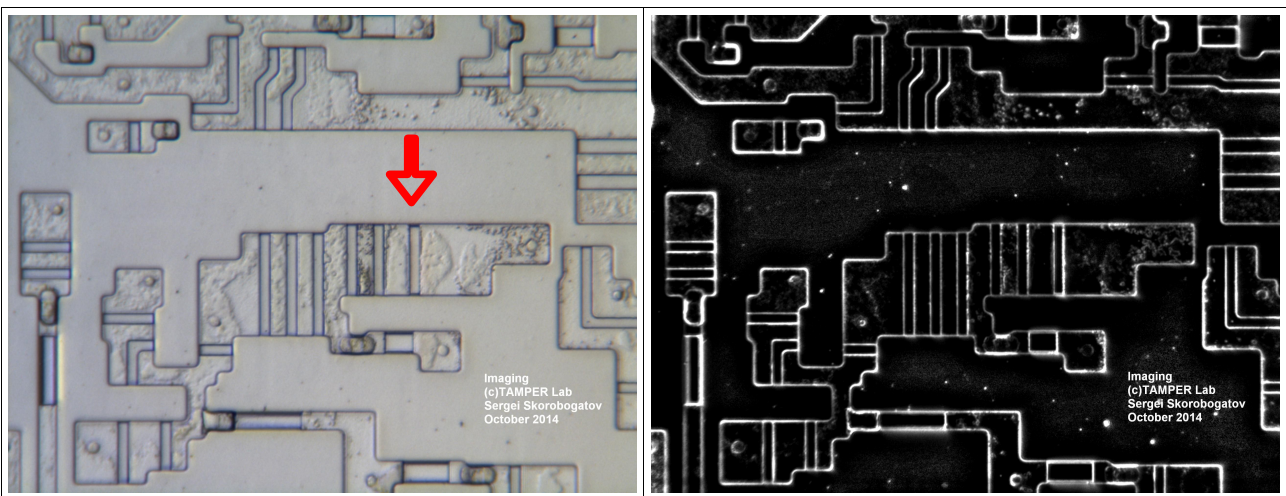


Fig.5. Brightfield and darkfield images with 50x objective of the transistor 3 area (top right corner).

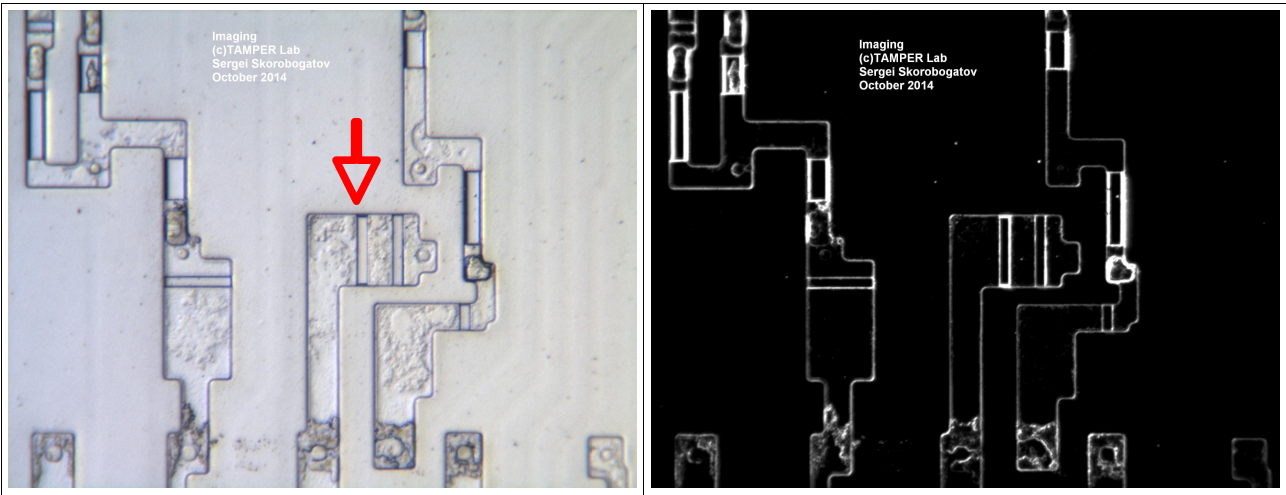


Fig.6. Brightfield and darkfield images with 50x objective of the transistor 4 area (centre).

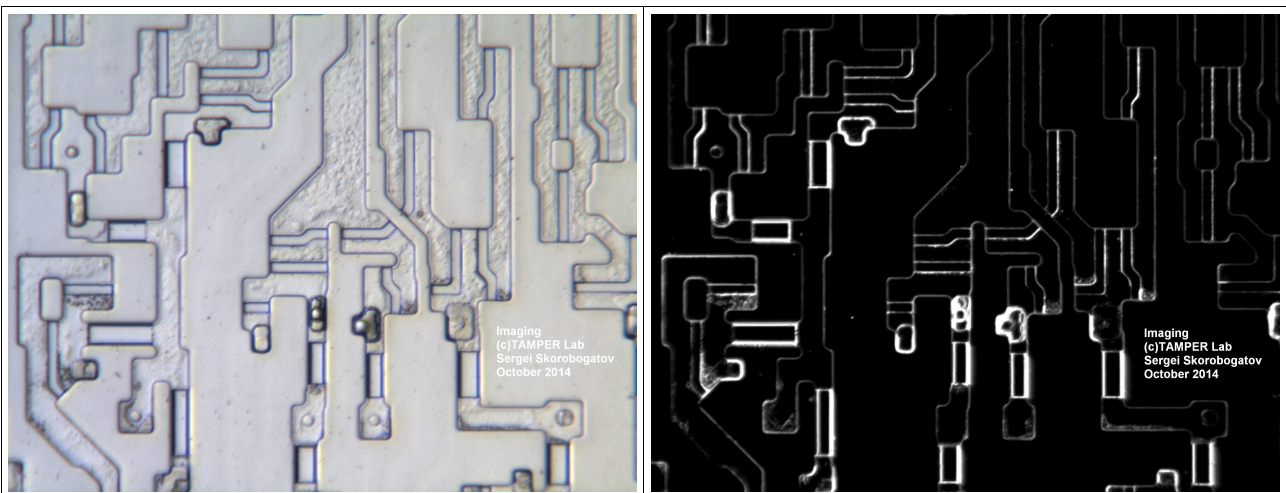


Fig.7. Brightfield and darkfield images with 50x objective of the transistor 5 area (middle left).

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Arrows added 11 November 2014